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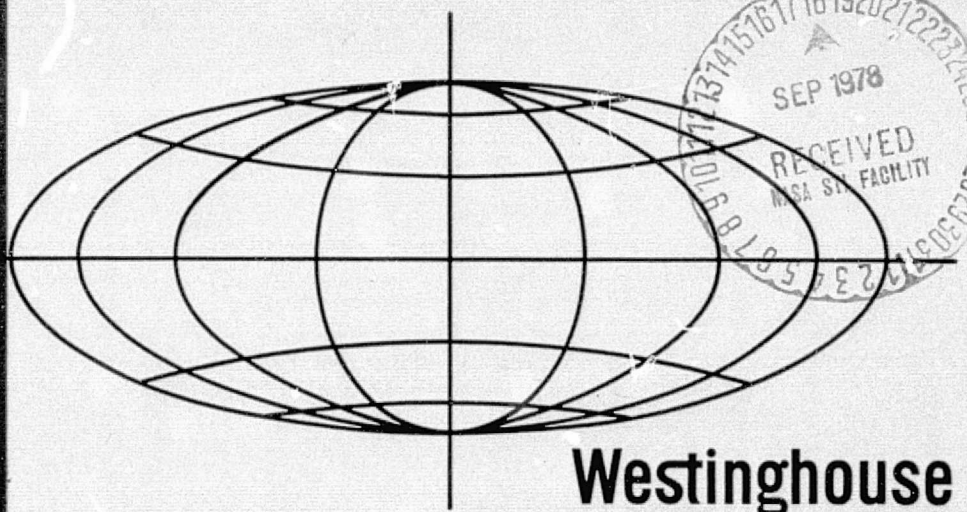
NASA CR-156807

TIME DELAY AND INTEGRATION ARRAY (TDI) USING CHARGE TRANSFER DEVICE TECHNOLOGY

Phase II Final Report

Volume I - Technical



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Time Delay and Integration Array (TDI) Using Charge Transfer Device Technology

Phase II Final Report

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Volume I - Technical

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TABLE OF CONTENTS

SECTION		PAGE
1.0	INTRODUCTION	1-1
2.0	SUMMARY	2-1
	2.1 Possible Future Development Work	2-5
	2.2 Performance of the Bench Test Equipment	2-6
3.0	TDI SENSOR DESIGN	3-1
	3.1 Processing Sequence For SnO Transparent Gate CCD's	3-14
4.0	TEST EQUIPMENT	4-1
	4.1 Chip Exerciser and Acquisition Interface Equipment	4-1
	4.1.1 Mechanical and Functional Description	4-1
	4.1.2 Modes of Operation	4-5
	4.1.3 Data Formatting - DTR	4-7
	4.1.4 Data Output Modes - DTR	4-9
	4.1.5 Software Description	4-11
	4.2 Correlated Double Sampling	4-14
5.0	DATA ANALYSIS	5-1
	5.1 Description of Tests	5-1
	5.2 Spectral Response	5-3
	5.3 Leakage	5-10
	5.4 Uniformity of Dark Level	5-11
	5.5 Signal-Noise Ratio	5-13
	5.6 Dynamic Range	5-18
	5.7 Linearity and Gain	5-20

LIST OF FIGURES

FIGURE		PAGE
2-1	PHOTOMICROGRAPH OF 20x9 TDI ARRAY	2-2
3-1	SYMBOLIC SCHEMATIC OF MSS MECHANICAL SCAN TECHNIQUE REFERENCE AXIS IS INCLUDED	3-2
3-2	SENSOR CHIP BLOCK DIAGRAM	3-3
3-3a	CROSS SECTION OF IMAGING PIXEL	3-5
3-3b	IMAGING PIXEL GEOMETRY	3-6
3-4	READOUT REGISTER CELL	3-7
3-5	OUTPUT STAGE	3-9
3-6	TOPOLOGICAL SCHEMATIC OF SENSOR	3-10
3-7	TIMING DIAGRAM	3-11
3-8	SELF-ALIGNED TRANSISTORS	3-17
4-1	CEAIE BLOCK DIAGRAM	4-2
4-2	CHIP TIMING	4-3
4-3	DTR SYNCHRONIZATION PULSES	4-10
4-5	FUNCTIONAL CTD-TDI SOFTWARE FLOW DIAGRAM	4-12
4-6	OUTPUT LISTING OF DATA REDUCTION PROGRAM	4-15
4-7	CORRELATED DOUBLE SAMPLING REMOVES RESET NOISE AT CCD OUTPUT	4-16
4-8	EFFECTIVE FREQUENCY RESPONSE OF A CDS SYSTEM	4-18
4-9	PHOTOGRAPH OF HYBRID, 4-CHANNEL ANALOG PROCESSOR	4-19
5-1	RELATIVE SPECTRAL RESPONSE OF CHIP 11-15	5-4
5-2	RELATIVE SPECTRAL RESPONSE BY ELEMENT	5-6
5-3	$NOISE^2$ VS ILLUMINATION	5-8
5-4	TDI SENSOR GAIN	5-19
5-5	NOISE VERSUS ILLUMINATION	5-21
5-6	DEVIATION FROM STRAIGHT LINE FITTED BETWEEN DARK AND MAXIMUM OUTPUT	5-22
5-7	DEVIATION VS ELEMENT	5-23

1.0 INTRODUCTION

This report covers Phase I and Phase II of a three phase program to design, fabricate, and test an image detection array using charge transfer device technology. The detector is an area mosaic array sensor of 20x9 detectors operated in a time delay and integration (TDI)* mode. The objectives of the three phases are:

Phase I - Device Design

Phase II - Fabrication and Flat Field Tests

Phase III - Dynamic Testing

The objectives of Phase I were achieved. More specifically these major technical accomplishments resulted:

- transparent, conductive SnO layers of 1.0 KÅ - 1.5 KÅ thickness
- multilayer SnO structures separated by SiO_2
- definition of SnO into line widths of 9.5 μm width and spacing
- low leakage ion implanted layer ~.2 μm deep
- operable CCD's with buried channels and transparent gates with transfer efficiencies >.999 at 1.25 MHz
- a sample 24x9 TDI array was fabricated
- a design was approved by NASA

The Phase II objectives of flat field testing was accomplished using two different techniques. A low frequency (79.2 μsec line time) correlated-double-

---

*See Appendix A for a detailed explanation of TDI operation.

sample was employed first. Since a great deal of experience has been gained previously in its operation, it was used to establish confidence in the device and demonstrate certain speed independent parameters. A bench test exerciser that operated at 8 μsec line time was fabricated and successfully operated the sensor. Feedthroughs of digital signals however precluded accurate measurements of dark level uniformity or noise. The characterization of the sensor indicated the following:

- Forward and reverse scan
- Uniform quantum efficiency greater than 60% from 400 to 850 nm
- Linearity better than 1%
- Noise performance within specification at proper well charge levels although at lower speed
- Dark level uniformity within specification at lower speed
- Functional performance at 1.25 MHz pixel rate and 8 μsec line time

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2.0 SUMMARY

The photomicrograph of Figure 2-1 shows the 20x9 TDI array (without light shield) which was developed to meet the Landsat Thematic Mapper requirements. This array is based upon a self-aligned, transparent gate, buried channel process that had been developed at Westinghouse. The process features: a) buried channel, four phase, overlapping gate CCD's for high transfer efficiency without fat zero; b) self-aligned transistors to minimize clock feedthrough and parasitic capacitance; and c) transparent tin oxide electrode for high quantum efficiency with front surface irradiation.

The requirements placed on the array and the performance achieved are summarized in Table 2-1.* This data is the result of flat field measurements only, no imaging or dynamic target measurements were made during this program. Measurements were performed with two different test stands, one fabricated on this program and one available for a short period at the Westinghouse Advanced Technology Laboratory. The bench test equipment fabricated for this program operated at the 8 μsec line time and employed simple sampling of the gated MOSFET output video signal. The second stand employed Correlated Double Sampling (CDS) and operated at 79.2 μsec line time. Although the correlated double sample test stand operated slower than required; spectral response, linearity, and detector gain should be unaffected when viewed at an equivalent charge level with respect to the 8 μsec line time.

*In the sections that follow TDI-3, TDI-6, TDI-9 will be referred to. These designations describe the number of stages of integration used to achieve different levels of gain. Specifically, TDI-3 implies three (3) stages of integration before readout. The other designations imply 6 stages and 9 stages of integration respectively.

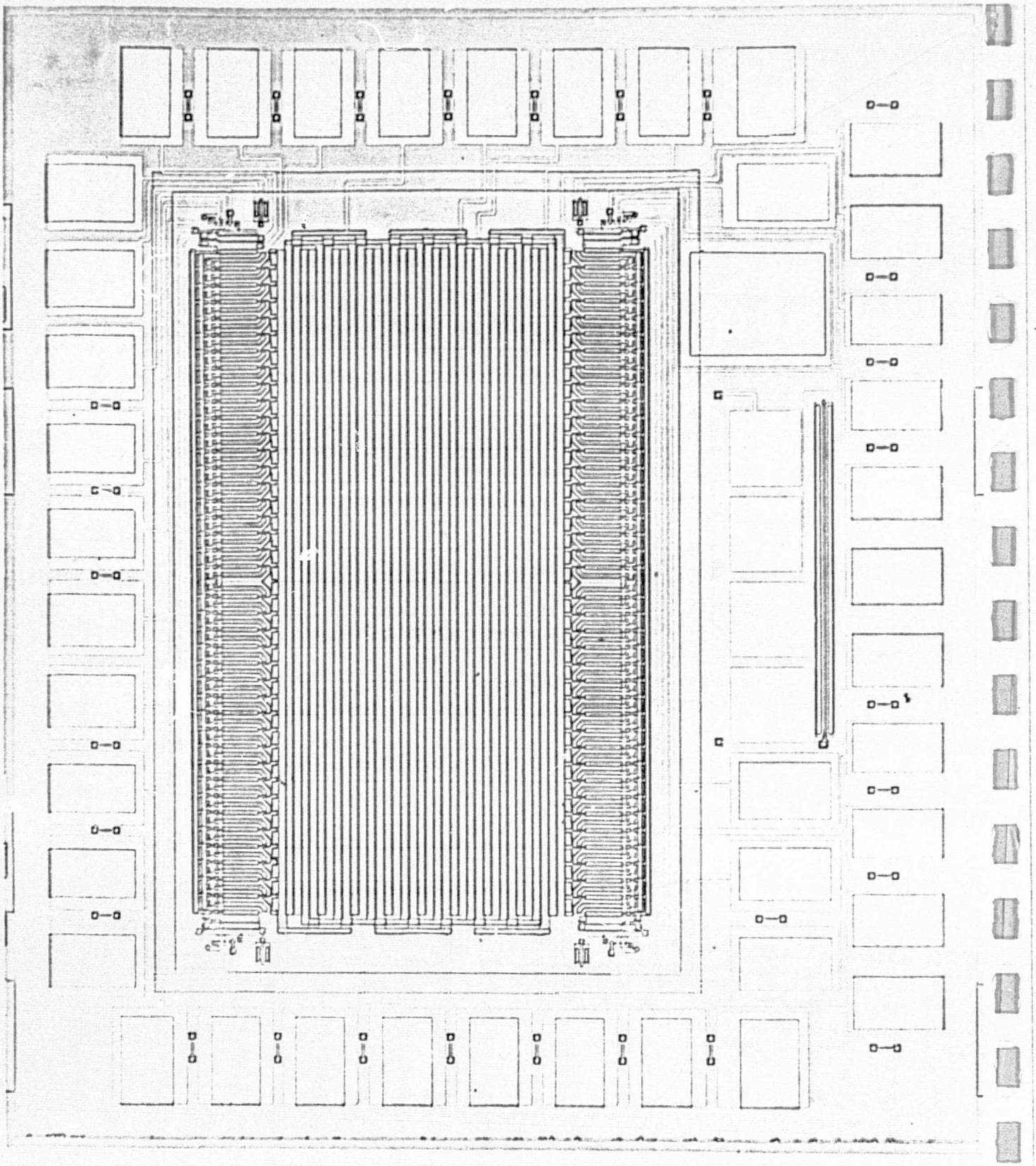

Figure 2-1. PHOTOMICROGRAPH OF 20x9 TDI ARRAY (without light shield)

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TABLE 2-1

REQUIREMENT		SPECIFICATION/ GOAL	DESIGN	REPORT REF.
Pixel Size		76 µm x 76 µm	76 µm x 76 µm	3.0
Number of Detectors				3.0
Across Scan (Y)		20	20	
Along Scan (X)		≤10	9	
Dwell Time		8 µsec	8 and 79.2 µsec	4.0
Spectral Response - max slope (%/µm)				5.2
Band #	λ(µm)			
0	.45 - .52	300%	214%	
1	.52 - .60	200%	150%	
2	.63 - .69	200%	100%	
3	.74 - .80	150%	167%	
4	.80 - .91	400%	155%	
Spectral Response - max ripple (%)				5.2
Band #				
0		5%	2.6%	
1		5%	1%	
2		5%	1%	
3		5%	1%	
4		5%	9%	

REQUIREMENT	SPECIFICATION/ GOAL	DESIGN	REPORT REF.
Signal-Noise			5.5
Band #			
0	105 @ .155 w/m^2		
1	145 @ .143 w/m^2	169-415 @ 15.7 mW/m^{2*}	
2	105 @ .087 w/m^2	30-55 @ 70 mW/m^{2**}	
3	85 @ .055 w/m^2		
4	120 @ .102 w/m^2		
Max Irradiance			5.6
Band #			
0			
1			
2		350 mW/m^2 @ 8 sec line time TDI-9	
3			
4			
Crosstalk			
Transfer Efficiency	.2%	No measurement	
Uniformity at Dark	10% max of band 2	7%*, 63%**	5.4
Uniformity of Gain		10%	5.7
Linearity(Deviation from best straight line)	3%	1%***	5.7

*TDI-9, 79.2 μsec line time

**TDI-9, 8 μsec line time

***(of max output deviation from straight line between dark and max output)

When viewed at specified charge levels and operated with CDS, the sensor achieved or exceeded specified performance except for minor deviations from the spectral response requirements. Measurements using the correlated double sample approach exceeded the required signal-noise ratio (SNR) at 6 stages of TDI. The specification would have permitted up to 10 stages of TDI in order to achieve the required SNR. The high speed bench test equipment did not achieve required SNR's, even at 9 stages of TDI. Section 5.5 of this report provides a detailed discussion of the measured signal-to-noise performance. It should be pointed out that even though the required SNR was exceeded using CDR signal processing, the theoretical noise limits predicted from a detailed noise model still were not approached. There appears to be either a design problem with the output CCD register or the fabrication process for this lot of wafers caused the output register and imaging section to have very high leakage current.

2.1 Possible Future Development Work

The results of these experiments suggest several possible directions of further development to improve signal-to-noise performance at the required line time. The first is to extend the correlated sampling technique to mega-hertz frequencies. This has already been employed in other applications at this laboratory although it has not been thoroughly evaluated. The second is to organize the sensor into sufficient parallel channels, thus lowering video bandwidth, and then integrate the correlated sample function on the sensor. Such an integrated processor has been fabricated, and initial test results indicate acceptable performance. The third is to employ a single

reset each line time, and use the output node as a signal summing device. Signal is recovered by differencing the output of adjacent pixel times. This differencing operation can be performed off chip in the analog domain or the digital domain. It is recognized that there will be dynamic range penalties, and it will be difficult to provide accurate high speed differencing.

These approaches are mentioned to suggest areas for modest near-term research and development activities to enhance the already demonstrated TDI results.

2.2 Performance of the Bench Test Equipment

Although this contract emphasized the development of the TDI array, a significant design effort was required to provide the high frequency timing to exercise the TDI array. Initially, C-V measurements on test SnO gate structures suggested the need for very versatile positive to negative voltage level clocks. In addition, a large number of modes of operation were desired. Rather than keep things simple the first time around, a calculated risk was accepted. The TDI device indeed operated under control of this sophisticated timing. However, a number of problems were never ironned-out in the time available under this contract, and therefore, ambiguous results were achieved at the megahertz clocking rates. The Phase III dynamic test program would have allowed these problems to be corrected.

3.0 TDI SENSOR DESIGN

The symbolic schematic as included in the specification of the Multi-Spectral-Scanner is shown in Figure 3-1. As the satellite proceeds in the Y direction due to orbital motion a scanning mirror nods and sweeps the image in the X direction across a line array of discrete TDI point detectors in the image plane. After scanning a swath across the surface of the earth the mirror is reset to its initial position to scan the next swath. Since mechanical motion is inherent in this application it is natural to take advantage of an area array operated in the time delay and integration mode (TDI) to improve the performance of the system as described in Appendix A. Future mechanical scanners will use image scan in both acrosstalk directions such as the current Landsat Thematic Mapper.

The block diagram of the TDI sensor fabricated for this program is shown in Figure 3-2. The sensor is an array of 20, 9 integration stage CCD's, operating in synchronism. The 20 channels are placed on the 76 μm centers in the Y direction. The 9 stages of each channel are also placed on 76 μm centers. At either end of the array and perpendicular to the channels is a readout register. The purpose of these readout registers is to receive the charge in a parallel fashion from the TDI channels and route it serially to the output node. Registers are provided at each end of the TDI channel such that by proper manipulation of the scan phases the array may be imaged in either direction of image motion. Each readout register is divided into 2 sections each of which receives the output of 10 of the TDI channels. The readout amplifier for each of the sections is at a corner of the array such that readout proceeds from the center outward. Thus there are four readout amplifiers on the chip, only

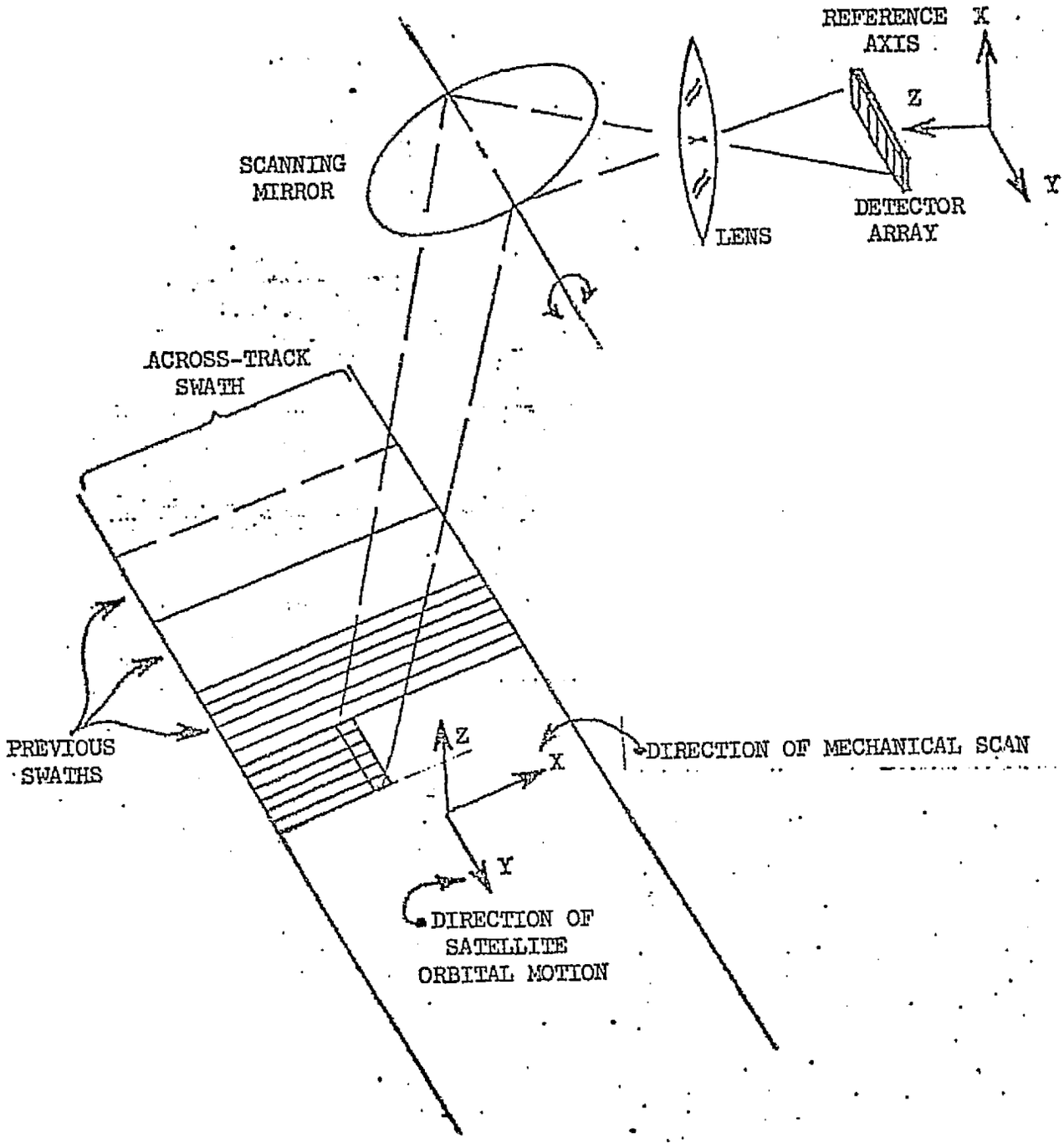

Figure 3-1. SYMBOLIC SCHEMATIC OF MSS MECHANICAL SCAN TECHNIQUE REFERENCE AXIS IS INCLUDED

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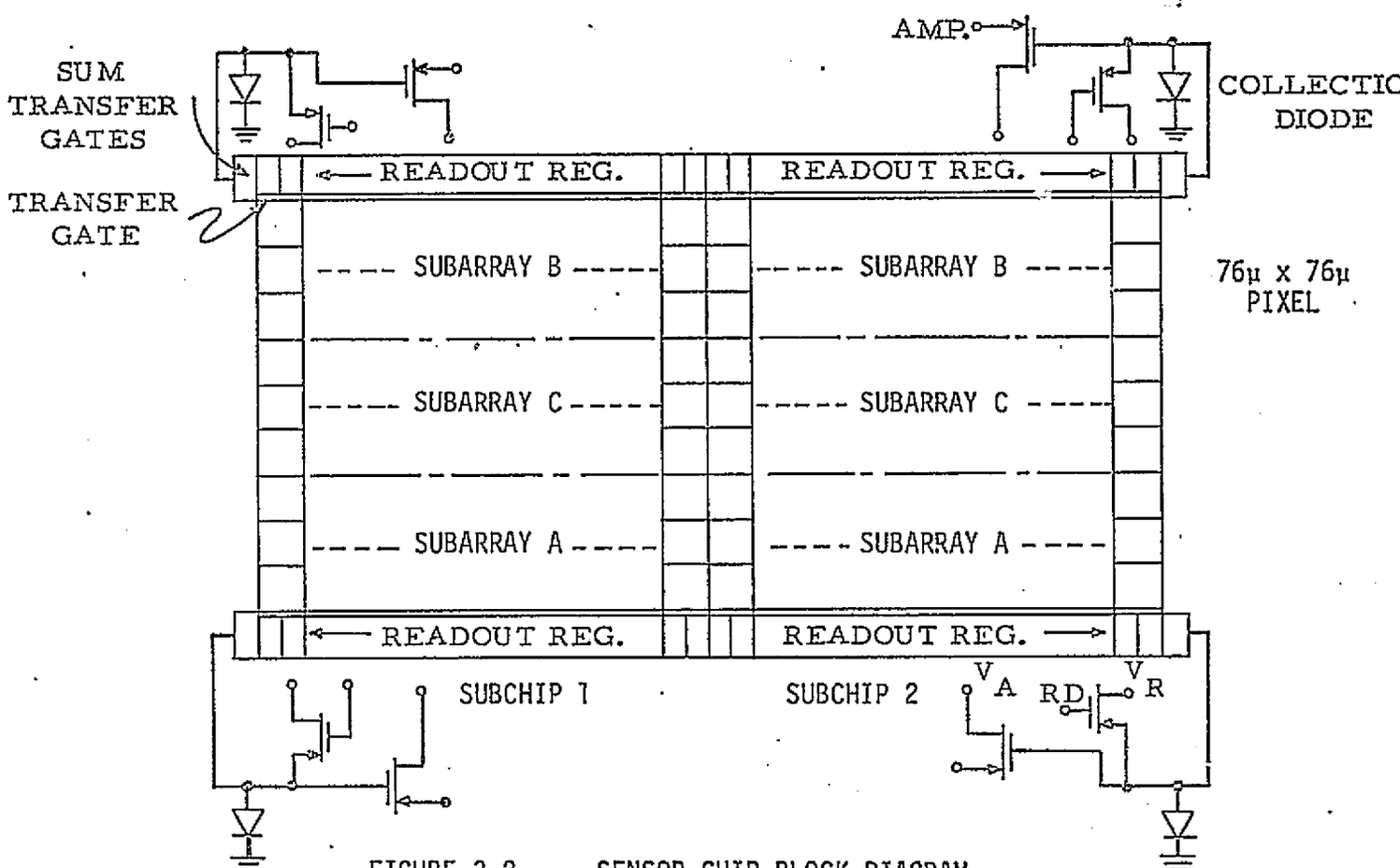

FIGURE 3-2. SENSOR CHIP BLOCK DIAGRAM

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two of which are receiving valid image data at any one time for a given direction of scan.

The array is divided into three independent sub arrays such that each TDI channel is divided into three sections of 3 pixels each. By control of the scanning pulses either one, two, or three of these sections are scanned in one direction while the remainder are scanned in the opposite direction. This creates a form of electronic exposure control which can yield an effective TDI of 3, 6, or 9 integration stages.

Figure 3-3 shows the layout of one pixel of the imaging array. The pixel is one cell of a 4 phase CCD constructed with transparent tin oxide electrodes. The cross section serves to illustrate the nature of the CCD construction while the top view illustrates the topological confines of the pixel. The basic charge transfer device is a 3000Å deep p-channel buried channel fabricated in a 10-20 Ω-cm ⟨100⟩ silicon substrate. The gate electrodes lie at two different distances from the silicon surface. The first is separated from the silicon surface by a dielectric layer consisting of 800Å of silicon dioxide and 400Å of silicon nitride. The second level of gates is separated from the first and the silicon surface by an additional 1500Å of SiO_2. The effective gate width of each of the gates is 19 μm with the second level having an additional 2 μm overlap of the first level gate on each edge. The imaging area is covered finally by 18 KÅ of deposited SiO_2, 10 KÅ undoped and 8 KÅ phosphorous doped.

Figure 3-4 shows the layout of 1 cell of the output register. Each cell consists of 8 phases which form 2 cells of a 4 phase shift register. The transfer gate effectively splits the output charge of the TDI column between the two cells. The output register is configured in this manner to reduce the transfer

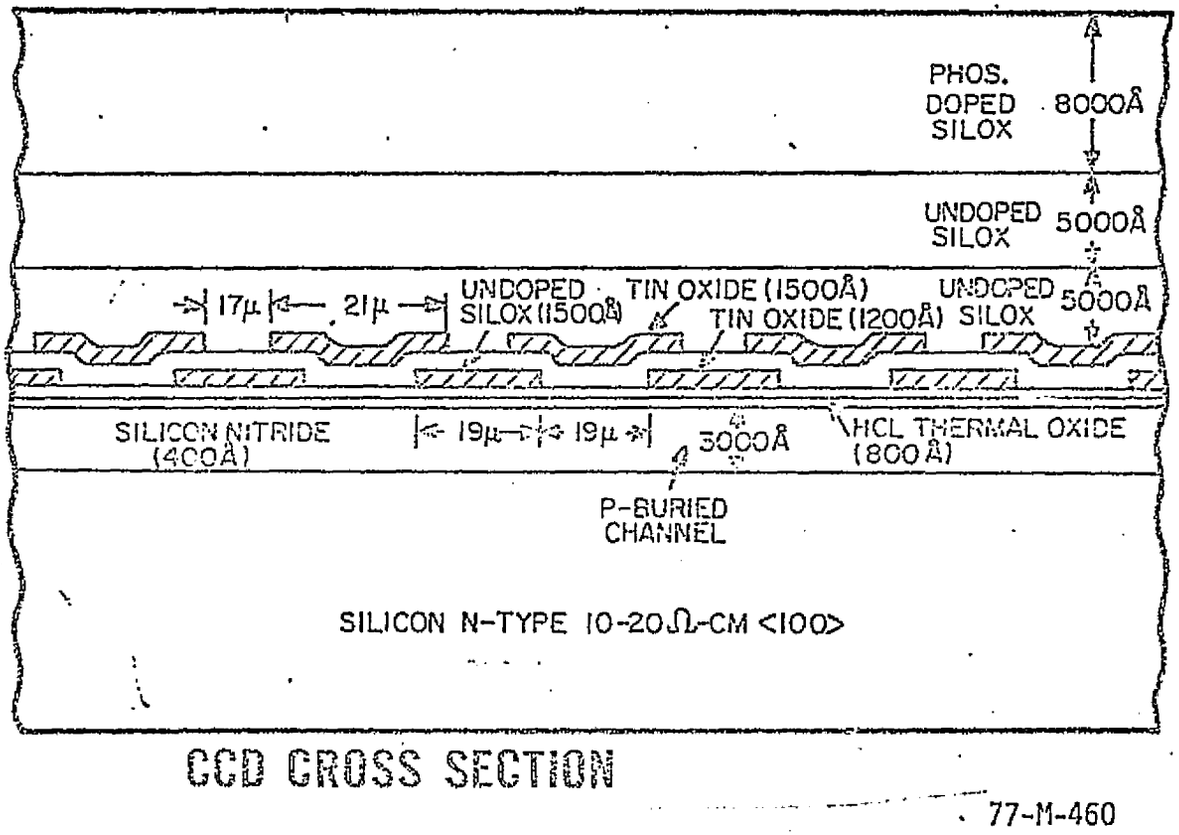

Figure 3-3a. CROSS SECTION OF IMAGING PIXEL

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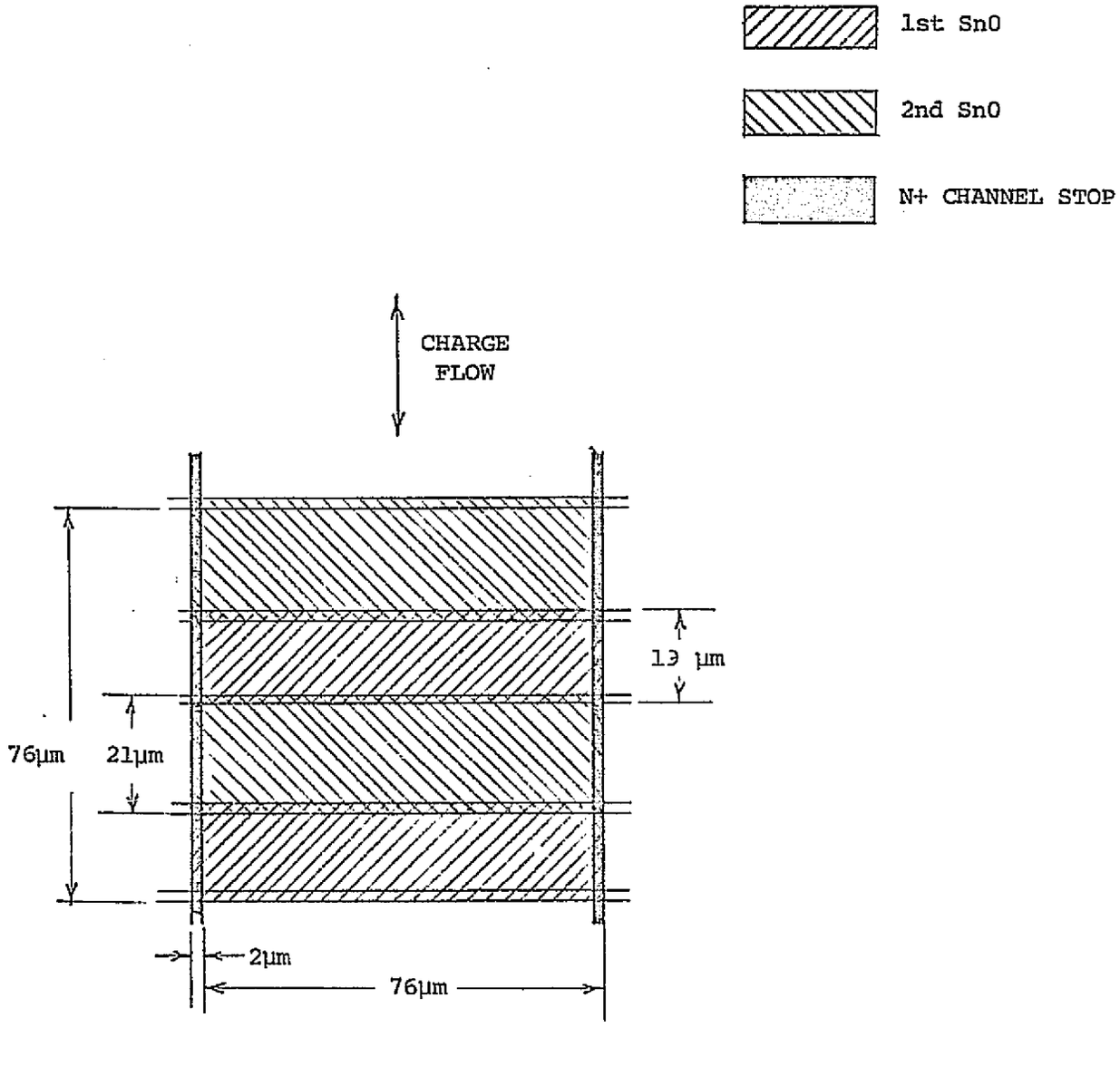

Figure 3-3b. IMAGING PIXEL GEOMETRY

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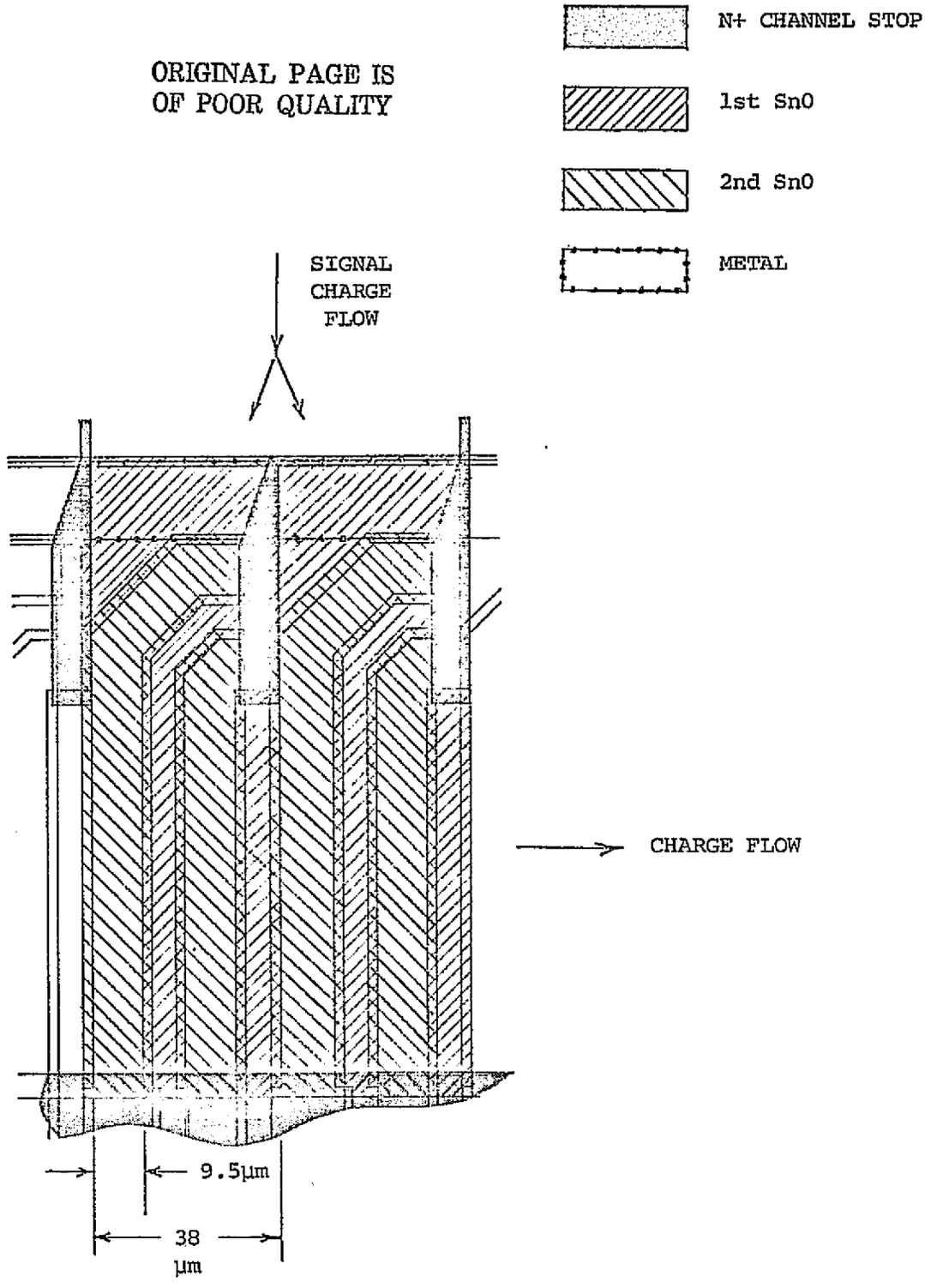

Figure 3-4. READOUT REGISTER CELL

length of the electrodes to 9.5 μm to provide higher transfer efficiency at the 8 μsec line time. The array is configured such that charge may enter the two Ø1 electrodes from 2 directions. One direction is via the transfer gate, and the other is from Ø4 of the contiguous stage. Ø1 and Ø2 are shaped like an inverted "J" such that charge has the same transfer distances during all movements no matter what position a charge particle may occupy under the electrode.

The output stage of the array is shown in Figure 3-5. It consists of 3 electrodes, a collecting diode, a reset switch, and an electrometer amplifier. The three output electrodes are a summing well, a transfer well, and a d.c. shield. The summing well is provided to receive the charge from two successive clock periods of the readout register and thus reconstructs the pixel output from each TDI channel. The transfer well enables the pixel charge to flow from the holding well. The d.c. shield serves to act as a shield to the output node from any pulse feedthrough from the transfer gate. The charge is collected on the output diode which is reset to a reference voltage after every pixel output. As the charge varies between pixels it will be reflected in variations of the output current of the FET which are in turn measured by the test equipment thus forming the electrical record of the output of each pixel. These signal variations are on the order of microamps to be detected out of a bias current of a milliamp.

Figure 3-6 is a topological schematic showing the physical relationship of the gates to one another and relating their name and position. The figure illustrates the one channel of the array, the readout register and the output detector. Figure 3-7 shows the timing pulses required to operate the array.

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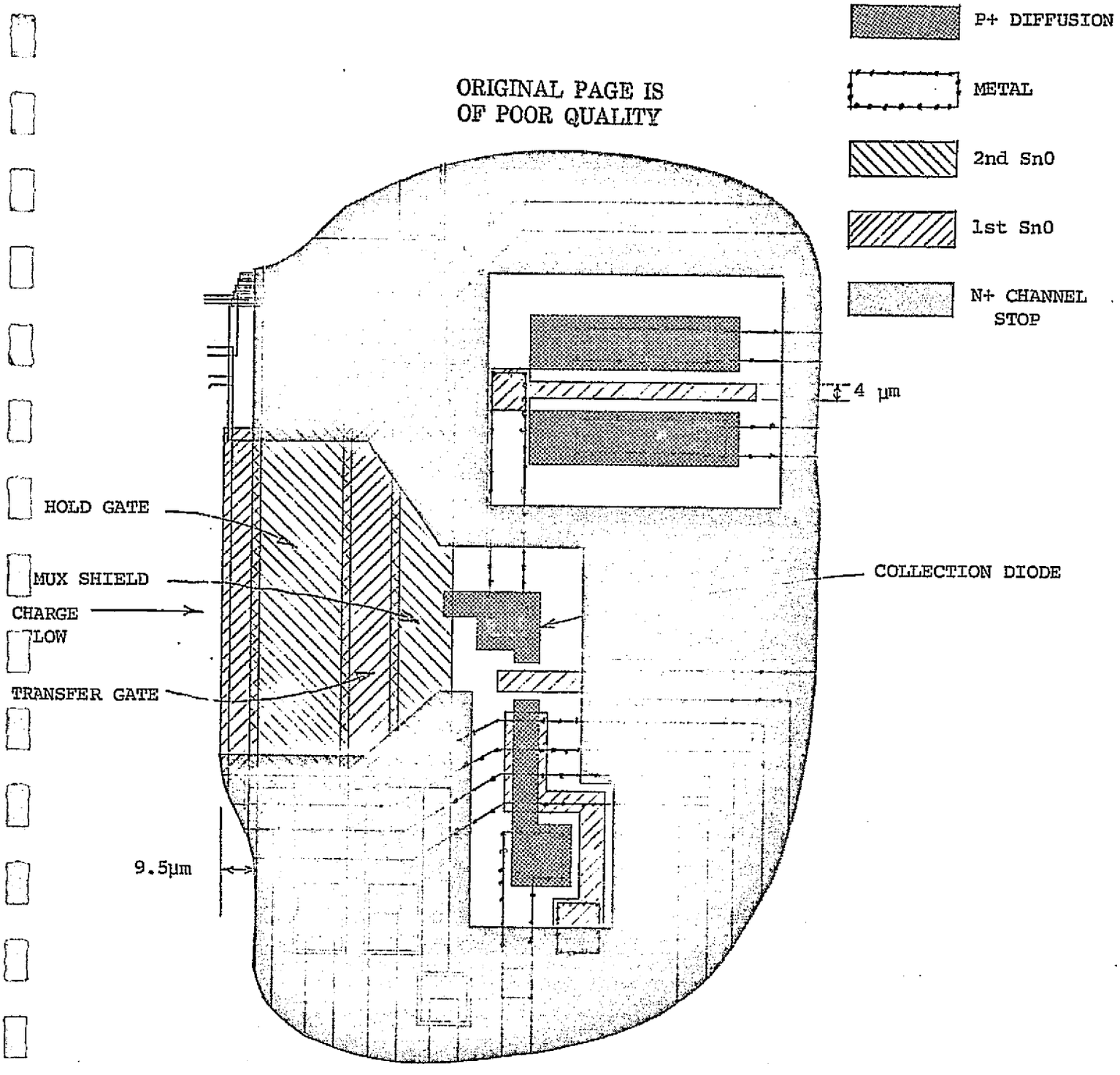

Figure 3-5. OUTPUT STAGE

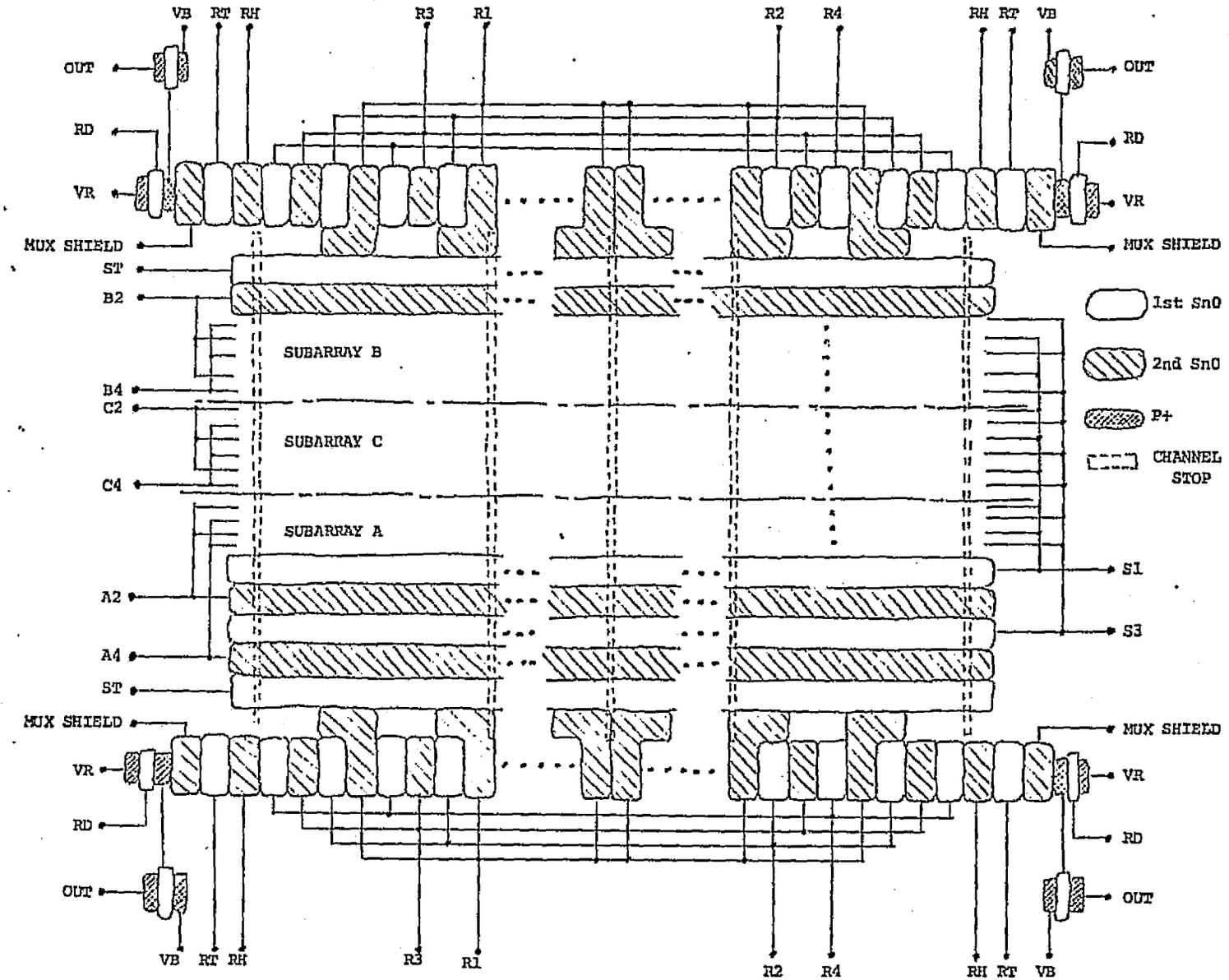

Figure 3-6. TOPOLOGICAL SCHEMATIC OF SENSOR

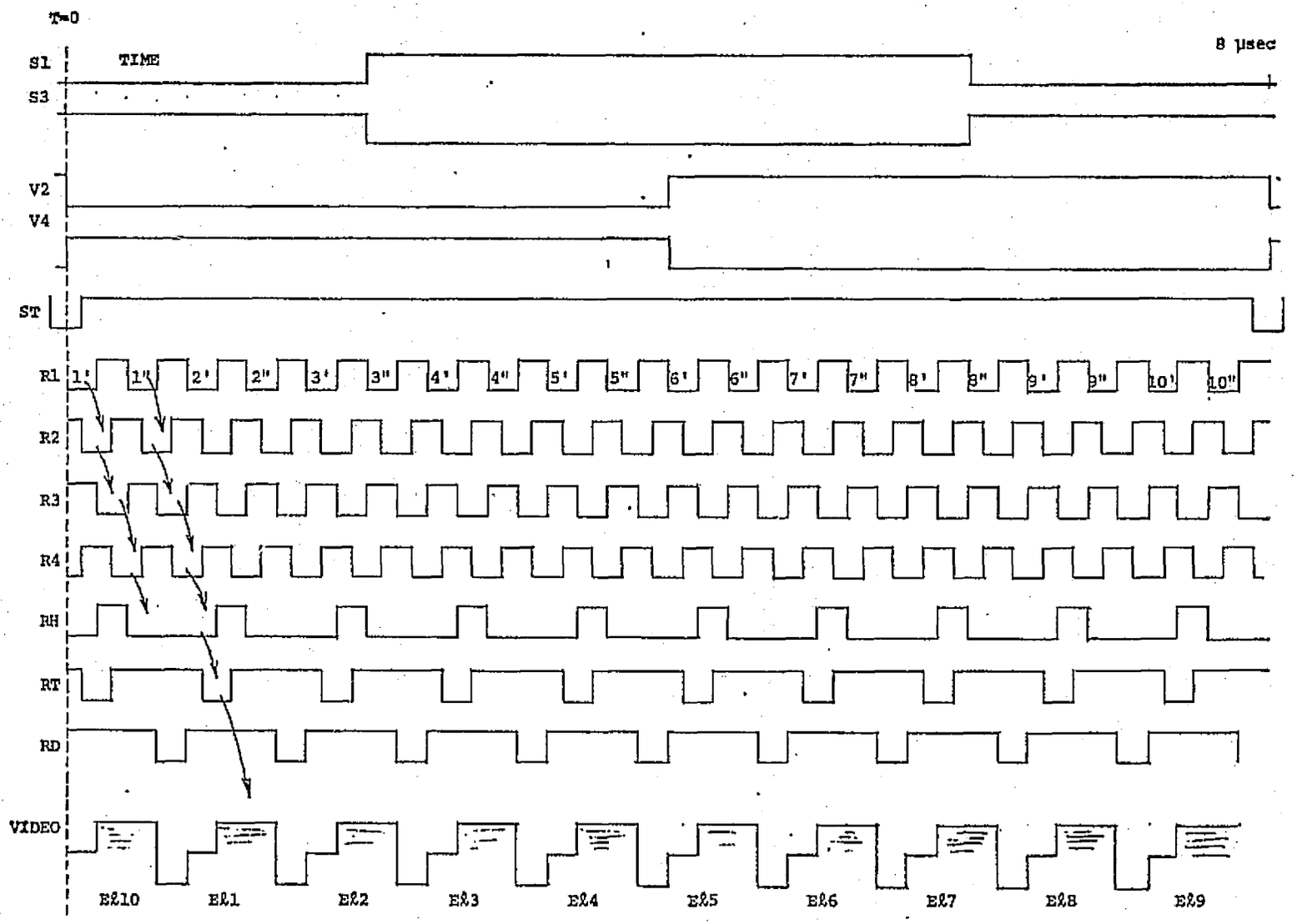

Figure 3-7. TIMING DIAGRAM

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The charge is transferred through the imaging section by the proper application of pulses S1, S3, V2, and V4. S1 and S3 are the same for all. V2 and V4 are applied to different gates as shown in Table 3-1 to control the mode.

To illustrate operation of the chip let us assume it is operating in the TDI-9 mode in which A2, B2, and C2 are tied to V2 and A4, B4, and C4 are tied to V4. Charge is contained under a gate when it is negative such that charge is first held under S1 and A2 when both are negative and then transferred to A2 and S3 as S1 voltage rises and S3 falls. As A2 rises and A4 falls charge is confined under S3 and A4, and then under A4 and S1 and so on until the charge reaches the last pixel before the readout register. At this point, the S3 voltage rise, and all the charge is confined under the A4 electrode. When A4 rises, the charge is transferred to the ST electrode which in turn transfers the charge into the two R1 phases of the readout register cell. Since all channels of the TDI array operate in synchronism at this point all cells of the output register have been loaded in parallel with their respective channel output charge.

The timing diagram of R1 thru R4 shows the charge under the four gates of the last readout register cell as a function of time. This timing is also common to all similar electrodes of the readout register on both ends of the TDI column. The charge is received by the R1 electrode and is moved through R4 and placed into the RH or holding well. After two cycles of R4 both halves of the charge from a TDI column have been placed in the RH well. It's voltage now rises transferring the charge to the transfer gate. While the holding gate voltage is high and blocking the transfer gate (RT) rises transferring the charge to the output diode thru the d.c. mux gate. Following this transfer of

TABLE 3-1

MODE PHASE CONTROLS

MODE	INTEGRATION TIME MULTIPLIER	A2	A4	C2	C4	B2	B4
Forward	1X	V2	V4	V4	V2	V4	V2
	2X	V2	V4	V2	V4	V4	V2
	3X	V2	V4	V2	V4	V2	V4
Reverse	1X	V2	V4	V2	V4	V4	V2
	2X	V2	V4	V4	V2	V4	V2
	3X	V4	V2	V4	V2	V4	V2

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charge (and prior to the next drop in the RT gate voltage to accept more charge), the reset switch is activated by a negative pulse to restore the diode to its initial condition. This operation is repeated, summing, transferring, and resetting, until all ten channel outputs have been read and the cycle is repeated.

To reverse the scan of the array phase V2 and V4 are interchanged such that A2, B2, and C2 are driven by V4 and A4, B4, and C4 are driven by V2. It will be noted that the array has only 8 S1 phases such that phase B2 is adjacent to the scan transfer gate on the opposite end of the TDI channel. Since the phase of B2 is now V4, charge will reverse its direction of flow. The readout register is identical to that on the other end of the array and operates in synchronism with it.

To achieve control of the number of TDI stages the clocks are manipulated as shown in Table 3-1. In essence if only 3 TDI stages are desired the remaining 2 sections of the column are clocked in the reverse direction thus routing their signal to the reverse readout register and output which is unmonitored. Reverse TDI control and TDI-6 are similarly created.

3.1 Processing Sequence For SnO Transparent Gate CCD's

The process sequence is given in Table 3-2. The starting wafers are 10 to 20 Ω-cm n-type ⟨100⟩ float zone silicon. An initial oxide of 10 KÅ of silox is deposited on the fronts and backs of the wafers. The low temperature silox in place of the usual thermal oxidation prevents formation of stacking faults on the silicon surface which can potentially cause high leakage. The first photo step is performed next to define P+ areas for contact to transistor source and drain regions. A boron diffusion and an oxide strip are per-

SELF - ALIGNED
TGATE PROCESS SEQUENCE

1. INITIAL OXIDE (10K FRONT/BACK)
2. PHOTO 1 (SOURCE/DRAIN DIFFUSION)
3. BORON DEPOSITION
4. BORON DRIVE/REOXIDATION
5. OXIDE STRIP
6. SILOX (10K FRONTS)
7. PHOS. GETTER
8. SILOX (15K BACKS)
9. ETCH FRONT OXIDE
10. OXIDATION (800Å)
11. PHOTO 2 (CHANNEL STOPS)
12. PHOS. IMPLANT (TWO STEP)
13. PHOTO 3 (BURIED CHANNEL)
14. BORON IMPLANT
15. RESIST STRIP
16. ANNEAL/OXIDE STRIP
17. GATE OXIDATION (800Å)
18. GATE NITRIDE (400Å)
19. FIRST TIN OXIDE (1000Å)
20. PHOTO 4 (FIRST GATE)
21. PHOTO 5 (SOURCE/DRAIN IMPLANT)
22. BORON IMPLANT
23. ANNEAL
24. SILOX (1.5K)
25. SECOND TIN OXIDE (1500Å)
26. PHOTO 6 (SECOND GATE)
27. SILOX (5K)
28. PHOTO 7 (VIA/CONTACT WINDOW)
29. BARRIER METAL DEP. (TUNGSTEN)
30. PHOTO 8 (BARRIER METAL)
31. PHOTO 9 (CONTACT WINDOWS)
32. INTERCONNECT METAL DEP. (ALUMINUM)
33. PHOTO 10 (INTERCONNECTS)
34. SILOX (5K UNDOPED + 8K DOPED)
35. PHOTO 11 (FIRST VIA)
36. LIGHT SHIELD METAL DEP. (ALUMINUM)
37. PHOTO 12 (LIGHT SHIELD)
38. SINTER

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formed next. Then 10 KÅ of silox is deposited on the fronts of the wafers and a phosphorous gettering diffusion is done into the backs of the wafers. Silox is deposited on the backs of the wafers to seal in the phosphorous and the oxide is removed from the fronts of the wafers. A 900°C thermal oxidation grows 800Å of oxide on the wafer fronts and the channel stop mask is photoengraved. A phosphorous ion implant forms the N+ channel stop regions on the wafers using the photoresist as a mask. The next mask is then applied to define regions for the buried channel. A boron ion implant forms the buried channel. The implant energy is 40 KeV and the dose is 2×10^{12}. The implants are annealed at 1000°C for 90 min to drive the buried channel into the silicon for about 5000Å. The wafers are then stripped of all oxide and the gate oxide is grown and the gate nitride is deposited. The first tin oxide layer is deposited using a CVD technique at 550°C. The first tin oxide clock lines are defined in the next photo step. The tin oxide is plasma etched and the photoresist is left on the tin oxide while the next mask is being applied. This mask opens windows over the transistor regions as shown in Figure 3-8. A boron ion implant then forms the self-aligned source-drain regions. After stripping the resist, a 1.5 KÅ 1% phosphorous doped silox is deposited as the insulator between the two tin oxide layers. Then the second tin oxide layer is deposited. Photoengraving and plasma etching define the second level tin oxide electrodes. A 5 KÅ undoped silox layer is deposited to insulate the tin oxide from the metal interconnect lines. The next photo step opens contact windows to the tin oxides as well as contact windows to the silicon. The via windows are etch-

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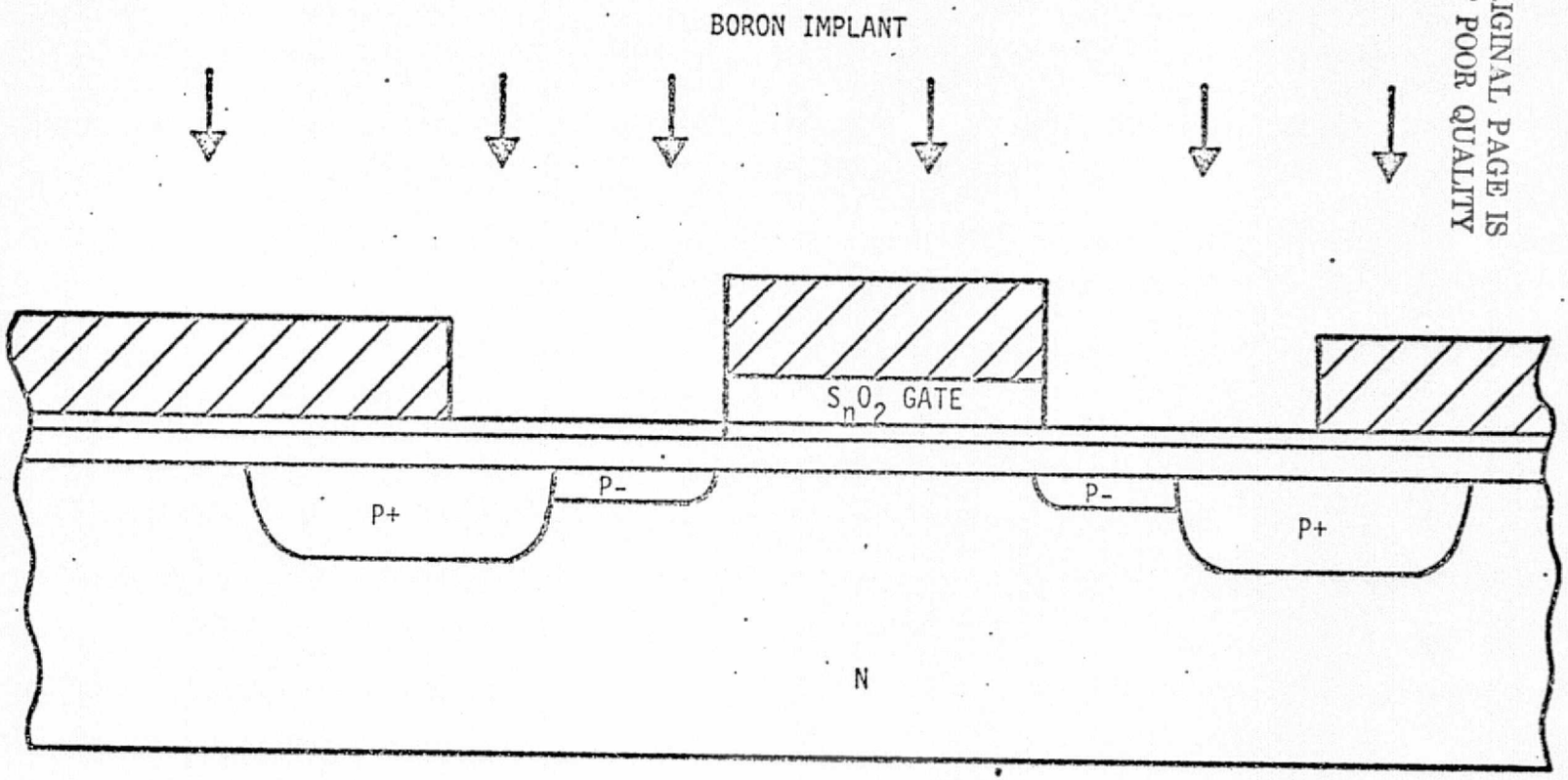

Figure 3-8. SELF-ALIGNED TRANSISTORS

77M-VA-035

ed in the silox down to the two tin oxide layers, while the contact windows are etched down to the gate nitride layer, since the nitride is not etched by the silox etchant. A 3 KÅ layer of tungsten is sputtered on the wafers and is then photoengraved so that tungsten only remains in the via windows. Tungsten is needed to make ohmic contact to tin oxide, but is not suitable for making contact to P+ silicon. Therefore, a tungsten-aluminum metalization system is used with the tungsten in the tin oxide via windows only. Following the photoengraving of the tungsten, the contact windows to the silicon are etched through the gate nitride/oxide layers. Aluminum is deposited and photoengraved to complete the first level interconnect system. Then 7 KÅ of silox and via windows are etched open down to the bonding pads. A second aluminum layer 10 KÅ thick is deposited and a light shield pattern is defined. The wafers are then sintered at 400°C for 30 min to complete the process.

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4.0 TEST EQUIPMENT

Two types of exercisers were used to acquire data on the TDI sensor. The first was fabricated on this program and operates the sensor at 8 μsec line time and 1.25 MHz pixel rate. The equipment simply samples the video portion waveform shown in Figure 3-7, converts the signal to digital form and stores the result on magnetic tape. The second employed correlated double sampling using a processor similar to that fabricated and shipped to NASA on contract NAS5-23856. An analog sample of the non-video portion of the waveform is subtracted from the video in the analog domain to form a new video which is converted to digital form and stored on magnetic tape.

4.1 Chip Exerciser and Acquisition Interface Equipment

The functions of the Chip Exerciser and Acquisition Interface Equipment, CEAIE, are to provide the timing signals and voltages required to exercise the chip, to sample the chip output and perform an analog to digital conversion, to format the digitized data, and to generate synchronization pulses for data acquisition by a digital tape recorder, minicomputer or bulk storage memory device.

4.1.1 Mechanical and Functional Description

The CEAIE physically consists of two assemblies, the control sole and the head, as shown in Figure 4-1.

The control console assembly consists of three functional subassemblies. They are 1) the digital logic unit, 2) the power conditioning unit and 3) the analog to digital converter unit. The digital logic unit contains the schottky and low power schottky circuitry required to 1) generate chip timing (see Figure 4-2), 2) generate timing for the A/D conversion, 3) format the digitized

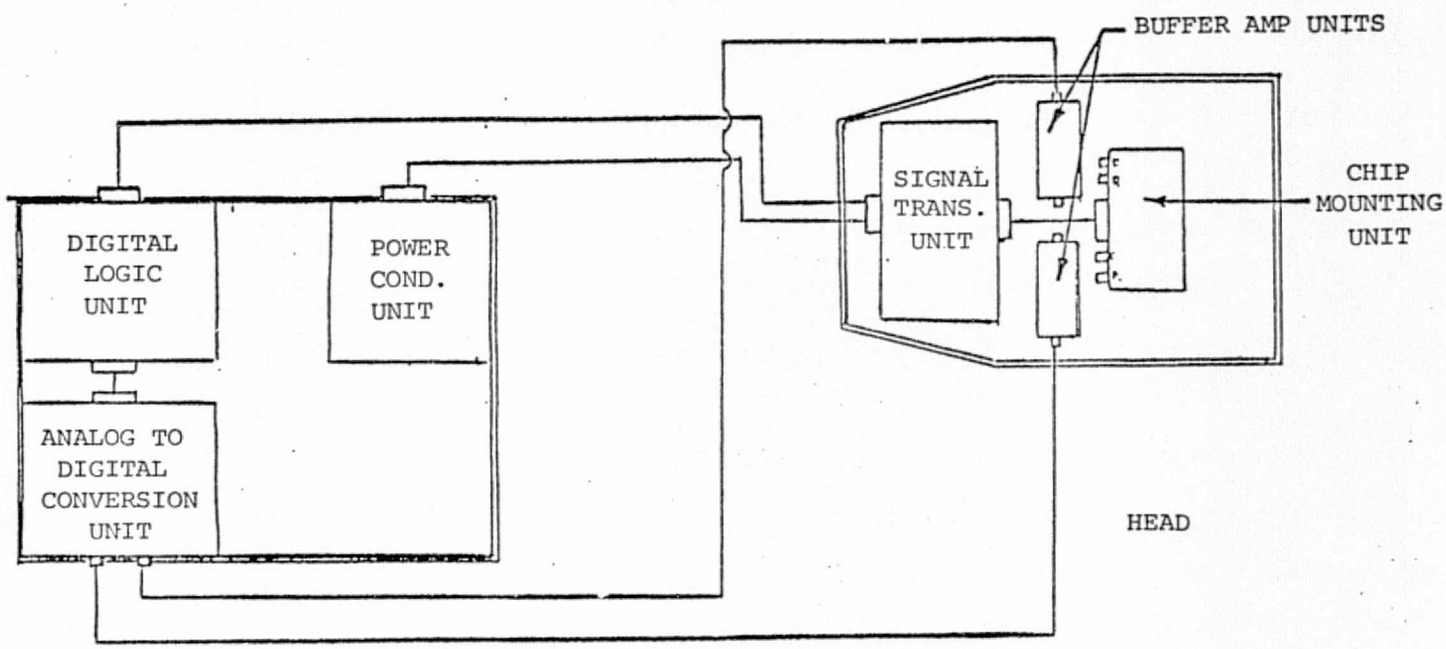


Figure 4-1. CEAIE BLOCK DIAGRAM

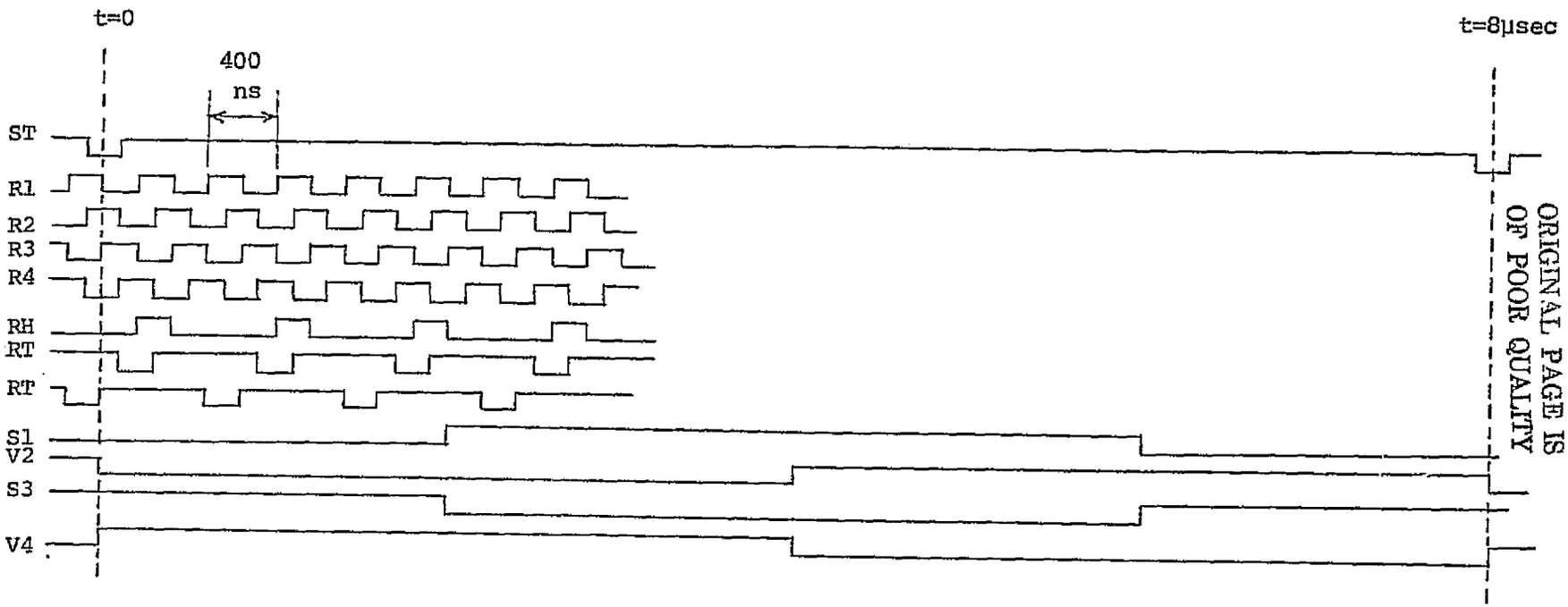


Figure 4-2. CHIP TIMING

chip output to be suitable for selected acquisition device, and 4) generate acquisition synchronization pulses. In addition, the digital logic unit contains the controls used to select the chip operating mode and data to be acquired. The power conditioning unit consists of adjustable, positive and negative power supplies. The power supplies are designed using solid state three terminal voltage regulators in conjunction with front panel mounted ten turn potentiometers. The positive and negative limits of the chip timing signals and the D.C. chip voltages are selected via the power conditioning unit. The range of the positive supplies is approximately -7V to +12V, while the range of the negative supplies is approximately -18V to +7V. The analog to digital converter unit consists of two identical printed circuit boards. Each board contains two A/D conversion channels and associated registers, multiplexers and drivers. An A/D conversion channel consists of a Datel SHM-5 sample and hold, an Analog Devices 50K operational amplifier and a Datel ADC-G10B3B ten bit analog to digital converter. Due to the conversion rate requirements the two A/D conversion channels on a board are time-shared and their output multiplexed. One of the boards services chip TDI channels 1-10, while the other board services channels 11-20. The outputs from both boards are transmitted over twisted pair cables to the formatting circuitry of the digital logic unit.

The CEAIE head assembly, which is designed to be mounted on an optical bench, consists of four subassemblies. The four subassemblies are the signal translator unit, the chip mounting unit and two buffer amplifier units. The signal translator unit utilizes the digital timing signals and limit voltages, output from the control console, to generate chip timing signals which swing between the limit voltages. This translation is accomplished by using

an HP5082-4364 optical isolators to drive a National semiconductor MH0007 MOS clock drivers. This translator configuration provides flexibility of the chip timing signals in that the high and low levels may both be positive voltages, both be negative voltages or the high level a positive voltage and the low level a negative voltage. The chip mounting unit consists of a 40-pin zero insertion force IC socket positioned on thermal electric device. The thermal electric device provides the capability to temperature cycle the chip. The chip outputs are transmitted over twinax cable to the buffer amplifier units. The two buffer amplifier units are identical, each containing an Analog Device 50K op amp. A ten turn potentiometer with calibrated knob allows the average current which must be supplied to the chip to be selected, thus providing adjustability of the dynamic range for the amplified chip output. The offset voltage at the inverting input of the op amp may be selected by adjustment of a trimmer pot. The outputs of the buffer amplifier units are transmitted over twinax cable to the analog to digital converter unit. In addition the outputs are also available on BNC connector for display on an oscillscope.

4.1.2 Modes of Operation

The CEAIE has the capability to exercise the chip in several modes of operation. The modes of operation are selectable from the front panel of the control console. These switches and their functions are discussed below.

CLOCK: INT/EXT

This switch allows the operator to vary the frequency at which the chip operates. The internal position provides the chip with a constant frequency generated by an internal oscillator. The external position allows an external frequency source to operate the chip.

DIR: F/R

This switch allows the operator to select the direction that the charge in the TDI section of the chip is transfered. The F position selects the forward direction while the R position selects the reverse direction.

X SELECT: MSB 1/0, LSB 1/0

These switches allow the operator to select the amount of time delay integration. The amount of time delay integration and the corresponding switch positions are shown in the following table.

TDI SECTIONS USED	LSB SWITCH POSITION	MSB SWITCH POSITION
A	0	0
A+B	1	0
A+B+C	0	1

MODE: NOR/LTI (PHASE: MSB 1/0, LSB 1/0)

These switches allow the operator to select between the normal integration time mode and the long term integration time mode. The long term integration time mode (LTI) stops the timing to the chip at any of the four phases of the TDI scan for a selectable time interval. After the time interval, normal clocking of the chip is continued. The TDI scan phase at which to stop the chip timing is selected by the PHASE: MSB and LSB switches.

The time interval that the chip clocking is stopped is settable by a dip switch inside the digital logic unit. The following table summarizes the use of the switches.

INTEGRATION TIME MODE	MODE SWITCH POSITION	PHASE SWITCH		CLOCK STOP TIME	
		LSB POS	MSB POS	NOR	FECP
NORM	NORM	N/A	N/A	N/A	N/A
LTI STOP ON Ø1	LTI	0	0	28ms-420ms STEPS OF 28ms	41ms-620ms STEPS OF 41ms
LTI STOP ON Ø2	LTI	1	0		
LTI STOP ON Ø3	LTI	0	1		
LTI STOP ON Ø4	LTI	1	1		

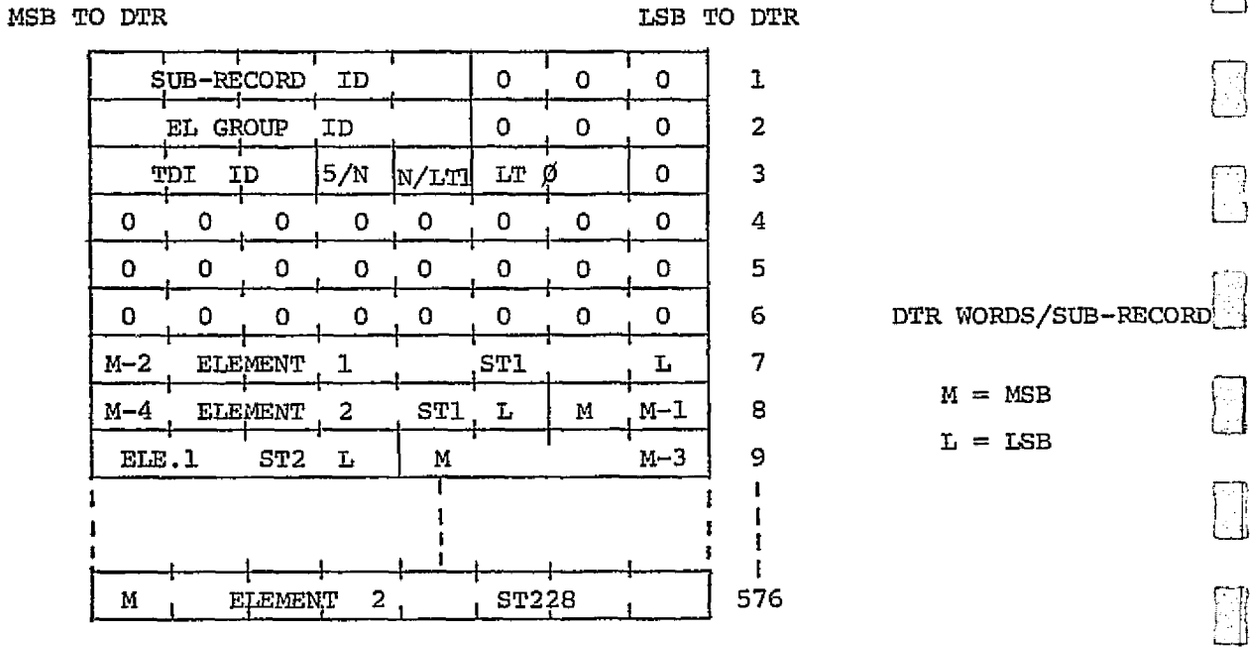
S/R MODE: NORM/FECP

This switch allows the operator to select the timing to the chip's output shift register. In the NOR position the chip will operate in it's normal mode. The FECP position causes the chip shift register to be clocked five extra times between scan transfers.

4.1.3 Data Formatting - DTR

The CEAIE is capable of formatting the chip output data such that it can be acquired on either a digital tape recorder (DTR), a minicomputer or a bulk storage memory device. Since the digital tape recorder has been the primary acquisition medium, the discussion of data formatting and acquisition will be thus limited. The CEAIE formatting section receives 10-bit words from the A/D

unit and generates 8-bit words co be transmitted to the DTR. This function is performed by a parallel to serial to parallel converter scheme. Two 10-bit words corresponding to two contiguous elements are converted per scan transfer time. The CEAIE transmits the data to the DTR in a sub-record format. The DTR combines two CEAIE sub-records to form a DTR record. A DTR file is composed of 20 CEAIE sub-records or 10 DTR records. Each CEAIE sub-record contains 576 eight bit words. The first six words are header, containing identification codes. The remaining 570 eight bit words are 228 ten bit element samples from each of 2 elements. The CEAIE sub-record composition is illustrated in the figure below.



Since a DTR record consists of two CEAIE sub-records, it contains 96 bits of header information plus 456 ten bit samples of each of two elements. Since a

DTR file consists of ten DTR records, it will contain 4560 ten bit samples of each of 2 elements or 456 ten bit samples of each of 20 elements. The synchronization timing provided to the DTR, by the CEAIE, is shown in Figure 4-3. This timing is initiated by the DTR ACQUIRE switch on the digital logic unit's front panel.

4.1.4 Data Output Modes - DTR

The CEAIE also provides the capability to select the data to be transmitted to the acquisition medium. The selection is accomplished by switches on the front panel of the digital logic unit. The function of these switches as applicable to DTR acquisition will be discussed.

MODE: AUTO/MAN (CHIP: 1/2 AND EL GRP/EL)

When the mode switch is in the AUTO position, the CHIP switch and EL GRP/EL thumbwheels are not functional. In this mode CEAIE will sequence through all 20 elements, two at a time, collecting 456 ten bit samples of each. When the mode switch is in the MAN position, the CHIP switch and EL GRP/EL thumbwheels are functional. In the manual output mode, 4560 samples of each of two elements are acquired. The elements to be acquired are selected using the CHIP switch and the EL GRP/EL thumbwheels. If the desired elements to be output are between elements one and ten inclusive the CHIP switch should be in the 1 position. If the desired elements to be output are between elements eleven and twenty inclusive the CHIP switch should be in the 2 position. With the EL GRP/EL thumbwheels the two elements to be output can be selected. The following table illustrates the two element combinations that may be selected.

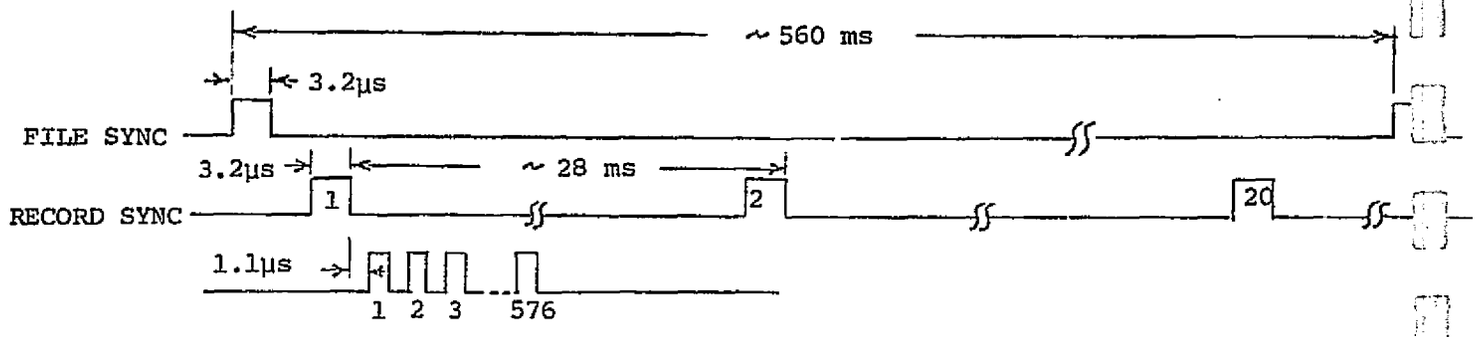


Figure 4-3a. (NORMAL)

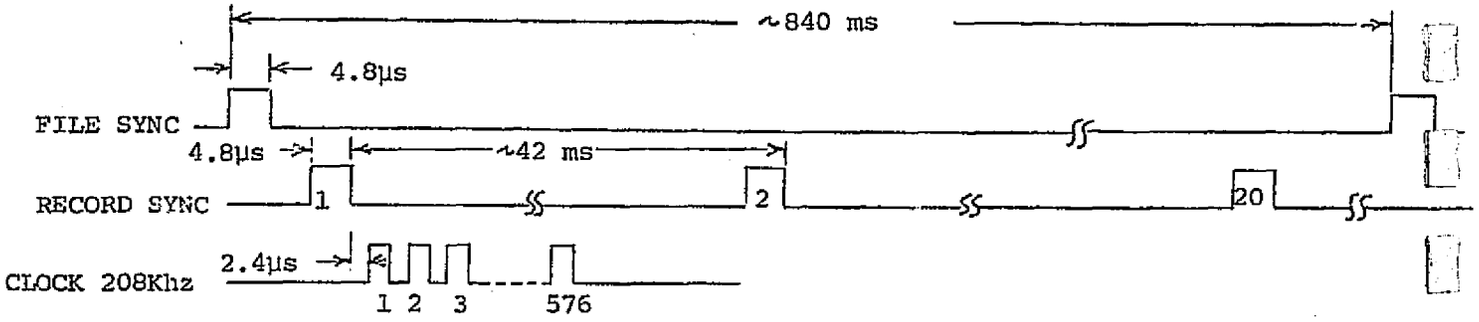


Figure 4-3b. (5 EXTRA CLOCK PULSES)

Figure 4-3. DTR SYNCHRONIZATION PULSES

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EL GRP POSITION	CHIP SWITCH POS.	
	1	2
0	10 & 1	20 & 11
1	1 & 2	11 & 12
2	2 & 3	12 & 13
3	3 & 4	13 & 14
4	4 & 5	14 & 15
5	5 & 6	15 & 16
6	6 & 7	16 & 17
7	7 & 8	17 & 18
8	8 & 9	18 & 19
9	9 & 10	19 & 20

ELEMENTS SELECTED

4.1.5 Software Description

Data taken from the sensor and placed on tape was compatible with a general purpose Univac 1110 computer on which reduction software was prepared. The software function was to reduce the data to suitable form for further analysis. Data was read from the DTR produced magnetic tape and "unpacked" into 10 bit words. The 456 samples of 20 TDI channels for up to 16 radiance levels were processed to obtain mean, standard deviation, responsivity, and SNR at each radiance level.

Figure 4-5 shows the functional flow diagram of the software. A library program for the 1110 was used to read each record into a computer buffer array. The buffer array consists of 257 - 36 bit computer words where each generated record contains 9216 bits. The header information which contains operating mode information is found in words 2, 3, 130, and 131. Word one contains data

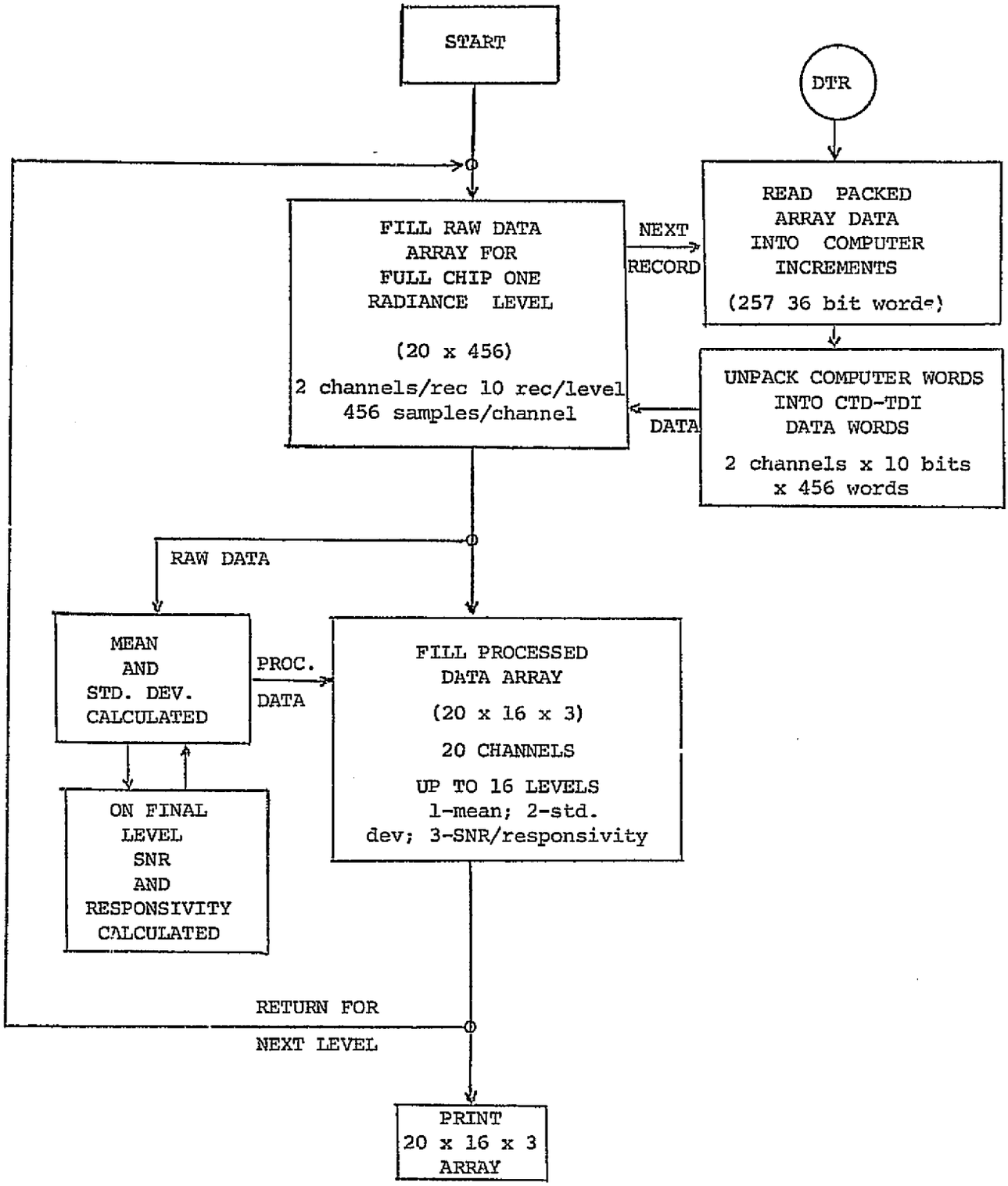

Figure 4-5. FUNCTIONAL CTD-TDI SOFTWARE FLOW DIAGRAM

and file numbers dialed into the tape recorder console. The remaining data in each record is 456 samples of 2 of the 20 TDI channels. The 10 bit data words are taken from the buffer and stored in a 20x456 word array for further processing.

The first processing step calculates the mean and standard deviation of each element using the relations below. Using this data a new 3 dimensional array is created containing the mean and standard deviation of each element of

$$\bar{X}_{ik} = \frac{1}{456} \sum_{n=1}^{456} X_{ikm}$$

$$\bar{S}_{ik} = \frac{1}{456} \sum_{n=1}^{456} X_{ir}^2$$

$$\sigma = \left\{ \bar{S}_{ik} - \bar{X}_{ik}^2 \right\}^{1/2}$$

where i = element number

k = radiance level

$\bar{X}_{ik}$ = element mean

$\bar{S}$ = sum of square

σ = standard deviation

the array at each of the radiance levels. The maximum number of levels is 16 with the actual number input as a data card with the program.

The gain (responsivity) factor is next calculated as the slope of a straight line through the maximum and minimum irradiance. At each level except dark a signal-to-noise value is calculated. These values are also placed in the data array.

The final function of the program is to format and print the data for each of the irradiance levels, an example of which is shown in Figure 4-6. First printed is a main header containing tape identification, mode identification, and chip number. This is followed by a listing of the mean, standard deviation, and signal-to-noise ratio of each element. The listing proceeds from the highest level to the lowest.

4.2 Correlated Double Sampling

There are four main noise sources that determine the signal to noise performance of this data: signal/leakage shot noise, Johnson noise of the reset switch, on-chip amplifier noise, off-chip amplifier noise. At low data rates, <1 MHz, the Johnson noise of the reset switch is the dominant noise source. Unlike other noise sources after the reset switch is opened the noise has been effectively sampled and held which results in a fixed but unknown initial condition before the receipt of signal charge. Correlated double sampling is a technique of measuring this initial condition and removing the uncertainty and hence this noise source from the video data.

A mechanization of correlated sampling is shown in Figure 4-7. After the reset switch has opened, a clamp switch closes at the output of the preamplifier to store the negative of the amplified reset noise charge on the coupling capacitor. The clamp switch then opens, sampling the electrometer and preamplifier transistor noise and holding this sample also on the clamp capacitor. The next signal charge packet is then transferred to the gate node of the on chip electrometer amplifier. The voltage at the preamplifier output is now the ampli-

FRAME 13 MM 7 DD 15 YY 77

SUB CHANNEL 0 CHANNEL 1 DIRECTION ~~REV~~

TDI SECTIONS 3 CLOCK MODE NORM OPERATING MODE TDI

DEVICE 5036, LOT 3453, WAFER 11 17

FFDATA LEVEL 1

ELEMENT	MEAN	STD DEV	SNR OR R(LAST LEV ONLY)
1	197.07	5.58	87.60
2	273.75	4.39	106.04
3	202.49	4.70	100.17
4	511.72	4.49	101.06
5	206.82	4.18	112.13
6	255.57	4.44	105.43
7	213.78	4.03	117.20
8	287.86	4.11	112.41
9	223.36	4.36	107.09
10	165.94	3.93	136.91
11	359.98	3.47	91.45
12	152.91	3.05	97.54
13	375.58	3.17	100.82
14	350.12	3.62	82.88
15	368.93	3.62	89.01
16	191.65	3.26	93.13
17	370.62	3.70	86.78
18	143.18	3.19	95.26
19	594.12	4.85	61.83
20	157.97	2.95	99.76

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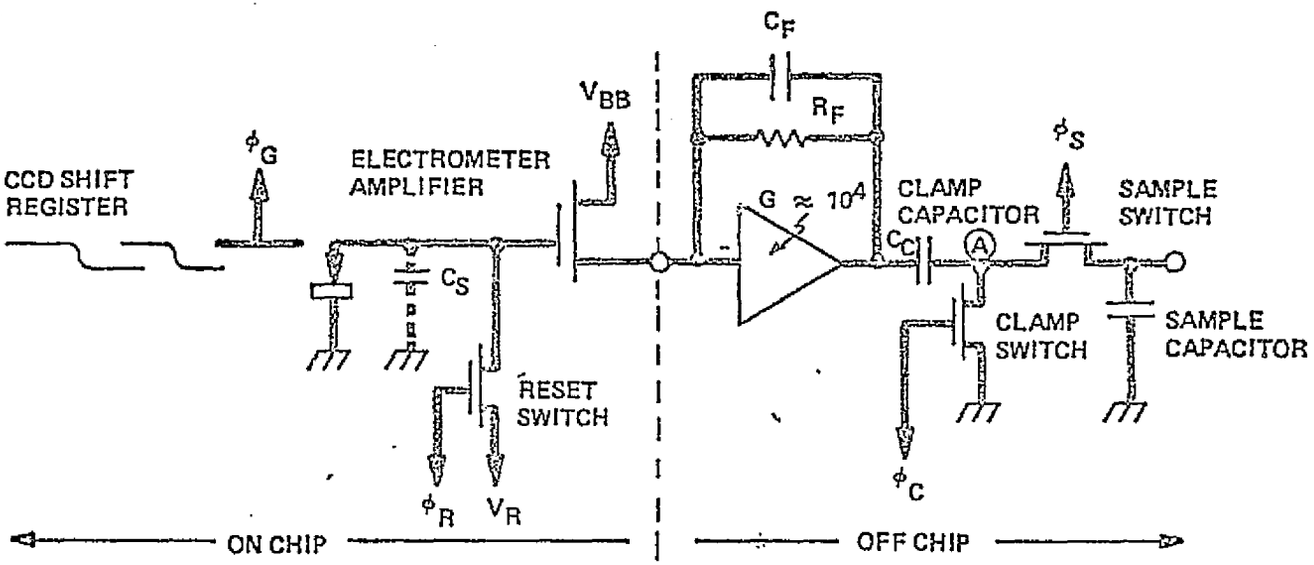
Figure 4-6. OUTPUT LISTING OF DATA REDUCTION PROGRAM



Reset switch replaces load resistor for CCD. Correlated double sampling shown removes most of reset switch Johnson noise, leaving CCD noise, electrometer amplifier noise, and off-chip amplifier noise. C_S is still a performance determining factor.

C.D.S. Operations:

1. Reset diode node to $V_R \pm \sqrt{kTC_S}$
2. Close clamp switch so negative of reset noise sample appears across C_C. Open clamp switch.
3. Transfer next signal charge packet to gated collection diode.
4. Signal at (A) is $f[(q_s + q_n) - q_n] = f(q_s)$ alone. Operate sample switch to present corresponding signal at output.

35-7440-VA-55

Figure 4-7. CORRELATED DOUBLE SAMPLING REMOVES RESET NOISE AT CCD OUTPUT

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fied signal plus the amplified reset noise plus the sampled transistor and amplifier noise plus the on going time varying transistor and amplifier noise. The voltage at the output of the clamp capacitor is the sum of amplified signal plus sampled electrometer transistor plus amplifier noise plus the on going transistor and amplifier noise. The reset noise has been removed. The transistor sample switch is then closed and opened, holding at the output the sum of the amplified signal plus two independent samples of electrometer transistor and preamplifier noise. The second amplifier noise sample was taken at the instant the sample switch was opened. As shown in the example, the reset noise was an order of magnitude larger than the amplifier noise and its removal is important despite the double sampling of amplifier noise.

Correlated double sampling has other advantages, however, since the clamp and sample operations are performed within a single element time, usually only one or a few microseconds apart. The system output voltage is the difference in instantaneous preamplifier output voltage between these two samples, which effectively provides ac coupling to neglect any frame rate or quasi-dc level shifts at the chip output. The effective frequency response of this system for a 2 microsecond delay between the opening of the clamp and sample switches is shown in Figure 4-8. The response at zero frequency is zero, and is very low at low frequencies to greatly reduce the effect of excess 1/f noise in the electrometer amplifier, the off chip preamplifier, the power supplies, or thermal variation of the on chip amplifier.

Figure 4-9 shows a processor built on contract NAS5-23856 which is similar to that used to test the sensor at a line time of 79.1 μsec. The processor is fabricated in a multichip hybrid package on a ceramic substrate using thin film gold interconnects. The amplifiers used are Westinghouse custom low power operational amplifiers, switches are RCA CMOS 4016. The unit shown consists of 4 channels contained in a 2" x 1" ceramic package with 68 pins.

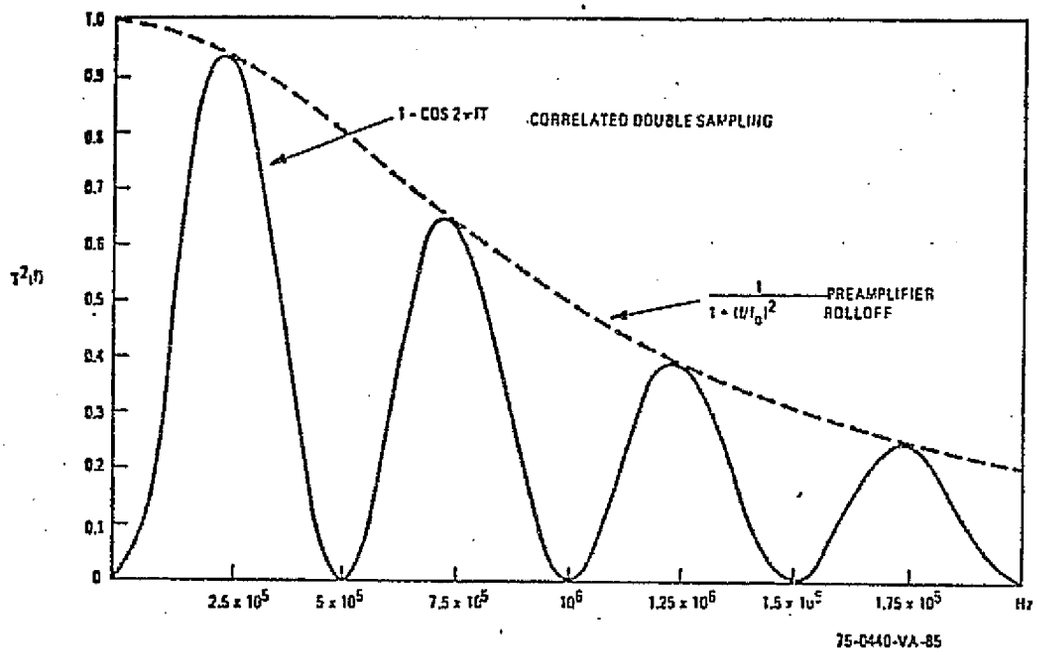

Figure 4-8. EFFECTIVE FREQUENCY RESPONSE OF A CDS SYSTEM WITH 2 µsec BETWEEN OPENING OF CLAMP AND SAMPLE SWITCHES

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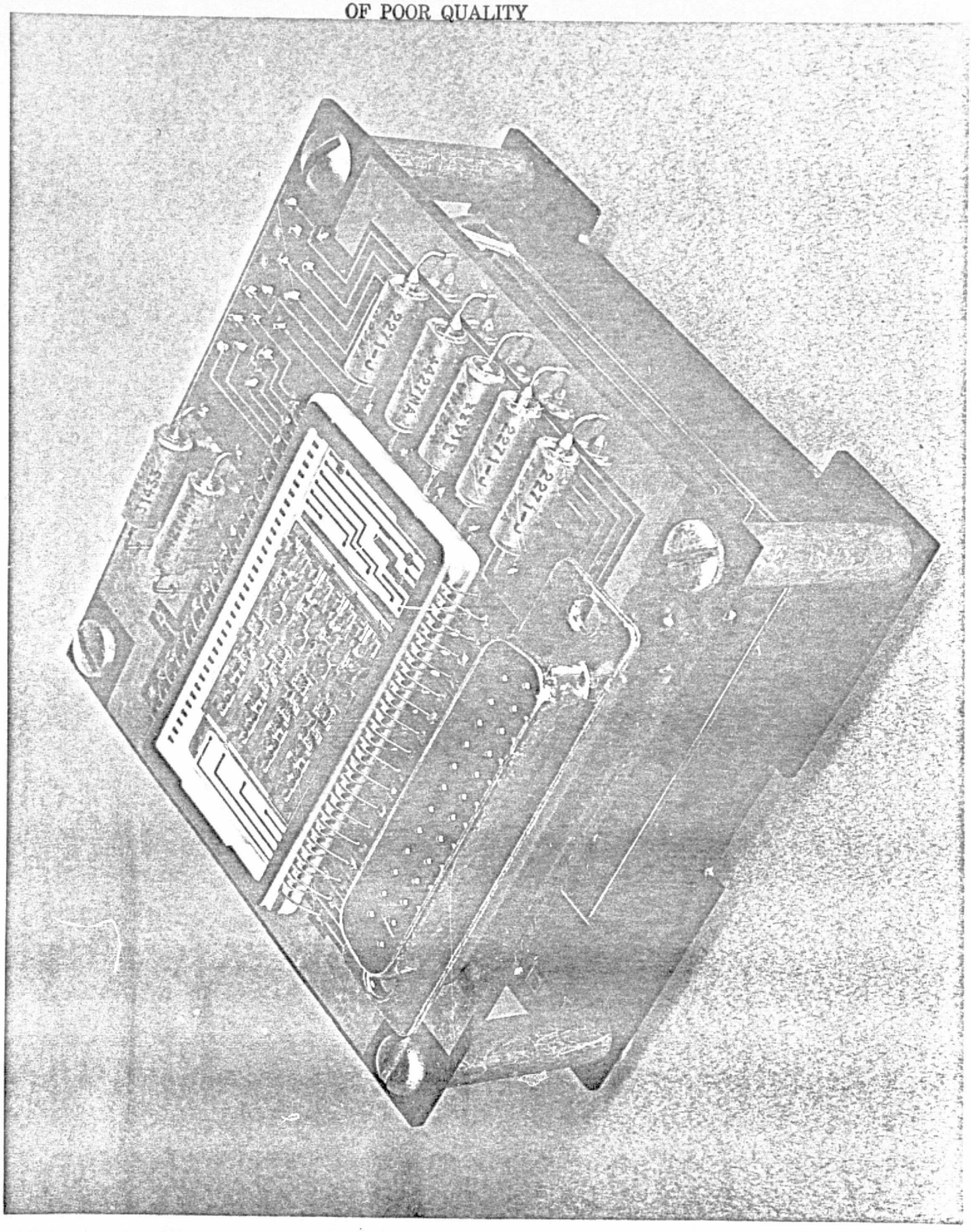


Figure 4-9. PHOTOGRAPH OF HYBRID, 4-CHANNEL ANALOG PROCESSOR

5.0 DATA ANALYSIS

5.1 Description of Tests

Since Westinghouse invented correlated-double sampling and has developed confidence in the results of this measurement technique, six chips were measured in this manner as a baseline for comparison with results measured by the high speed test equipment. The correlated double sample measurements were made at 79.2 μsec line time as opposed to the 8 μsec line time of the high speed test equipment. The 79.2 μsec line time, approximately an order of magnitude longer than system requirements, colors the data in two ways. First, it allows leakage shot noise to be a dominant factor in the dark level noise. Second, all amplifiers have a smaller bandwidth, which effectively lowers their noise contributions. Spectral response, linearity, dynamic range (in equivalent charge), and gain uniformity may, however; be reasonably measured at this lower speed. The data must be analyzed at equivalent charge levels for comparison, i.e., the charge level in the CCD well at 15.7 mW/m^2 and 79.2 μsec line time is the same as that at 155 mW/m^2 and 8 μsec line time.

The tests performed using the correlated double sampler are summarized in Table 5-1. Each test at a TDI level was made at 14 levels of illumination band limited to the 400 - 800 nm range of a 6000°K black body. The spectral tests consisted of measurements of response to 16 spectral bands plus a measurement of the dark output. The leakage measurement consisted of the measurement of the dark output of first TDI-9, then TDI-6, TDI-3, and finally of the read out register alone. All of the measurements consisted of 256 samples of the output of each sensor on the chip.

The detailed data from these tests are included as Volume II, and only a summary is provided in the various parts of this section. For each sensor

TABLE 5-1

CHIP #	FORWARD TDI-3	TDI-6	TDI-9	LEAK.	REVERSE TDI-3	TDI-6	TDI-9	LEAK.	SPECTRAL FOR TDI-9
11-1	X	X	X		X	X	X		X
11-5	X		X	X	X			X	X
11-3	X		X	X	X			X	X
11-7	X		X	X	X			X	X
11-17	X		X	X	X			X	X
11-13	X	X	X		X	X	X		X

chip and TDI the mean output of the 256 samples of each element are listed for each light level. The standard deviation is also listed for each element at each light level. For the spectral test, the mean output of each element at each wavelength is listed. In addition, the deviation of the signal from a straight line between dark and maximum illumination was calculated for each element for all tests of chips 11-1 and 11-5 and for 4 elements at each level for the other chips. The relative spectral response of all elements was calculated for each element of chips 11-1 and 11-5 and for 4 elements each for the remaining chips. During these tests the correlated double sample unit operating characteristics remained unchanged except for an output attenuation of $\sim$2X for TDI-9 measurements of sensors 11-7, 11-17, and 11-1.

A very limited amount of data was taken at 8 μsec line time. Included in Volume II is a set of measurements on sensor 11-17 at 6 light levels plus dark, TDI-9, forward and reverse. In addition a set of measurements at dark for the three TDI modes forward and reverse was taken to assess the leakage effects. More complete measurements were planned for the third phase program (not funded at the time of this report).

5.2 Spectral Response

The spectral response measurement consists of measurements at 16 spectral bands plus dark. The spectral bands have a 50 nm halfwidth with centers and irradiance as shown in Table 5-2. The irradiance at each wavelength is

TABLE 5-2

WAVELENGTH (nm)	IRRADIANCE (mW/m^2)
376	14.057
430	2.957
473	3.192
528	2.664
571	2.761
624	2.156
678	2.131
719	2.119
774	1.683
830	2.037
876	2.285
924	2.553
981	3.997
1019	6.473
1081	16.149
1130	49.162

weighted inversely proportional to the expected spectral response of the sensor. This was done such that the sensor is always operating at a nominal output current so that nonlinearities of the output do not cause errors in the spectral response measurements.

Figure 5-1 shows the relative spectral response of chip 11-5. The solid line is the mean of the entire chip and the dashed line shows the maximum devi-

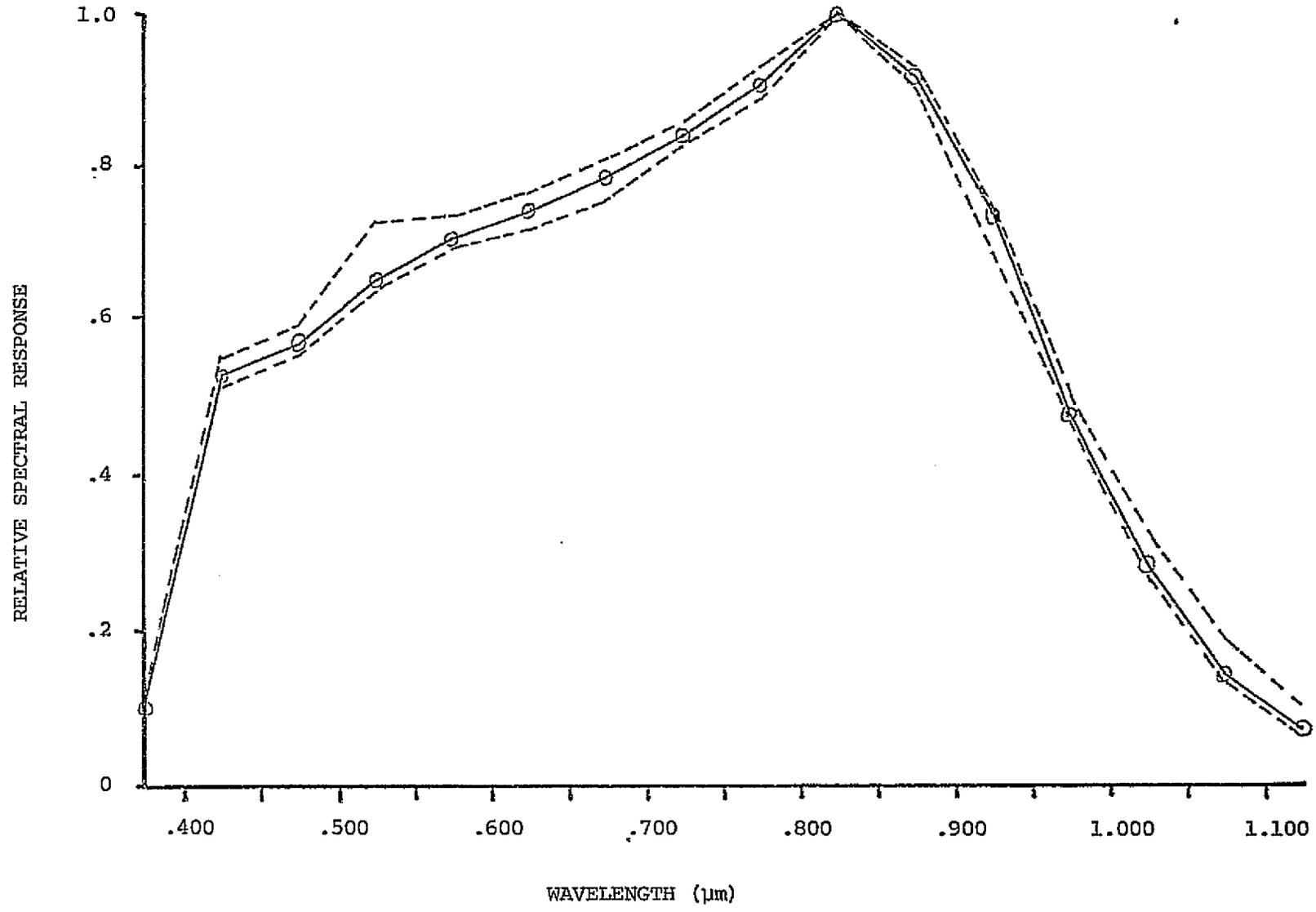


Figure 5-1. RELATIVE SPECTRAL RESPONSE OF CHIP 11-5

ation from the mean. Figure 5-2 is a plot the relative spectral response by element at 981, 774, 528, and 376 nm. In all cases the deviation among elements and the deviation from the mean spectral response of the chip is no more than 10% of full scale. The spectral characteristics of this chip are summarized in the table below. These parameters are all within specification except the ripple in the 800-900 nm band and the slope on the 740-800 nm band. The minimum

TABLE 5-3

BAND (nm)	SLOPE (%/μm)	RIPPLE (%)
.450 - .520	214	2.6
.520 - .600	150	1
.630 - .690	100	1
.740 - .800	167	1
.800 - .910	155	9

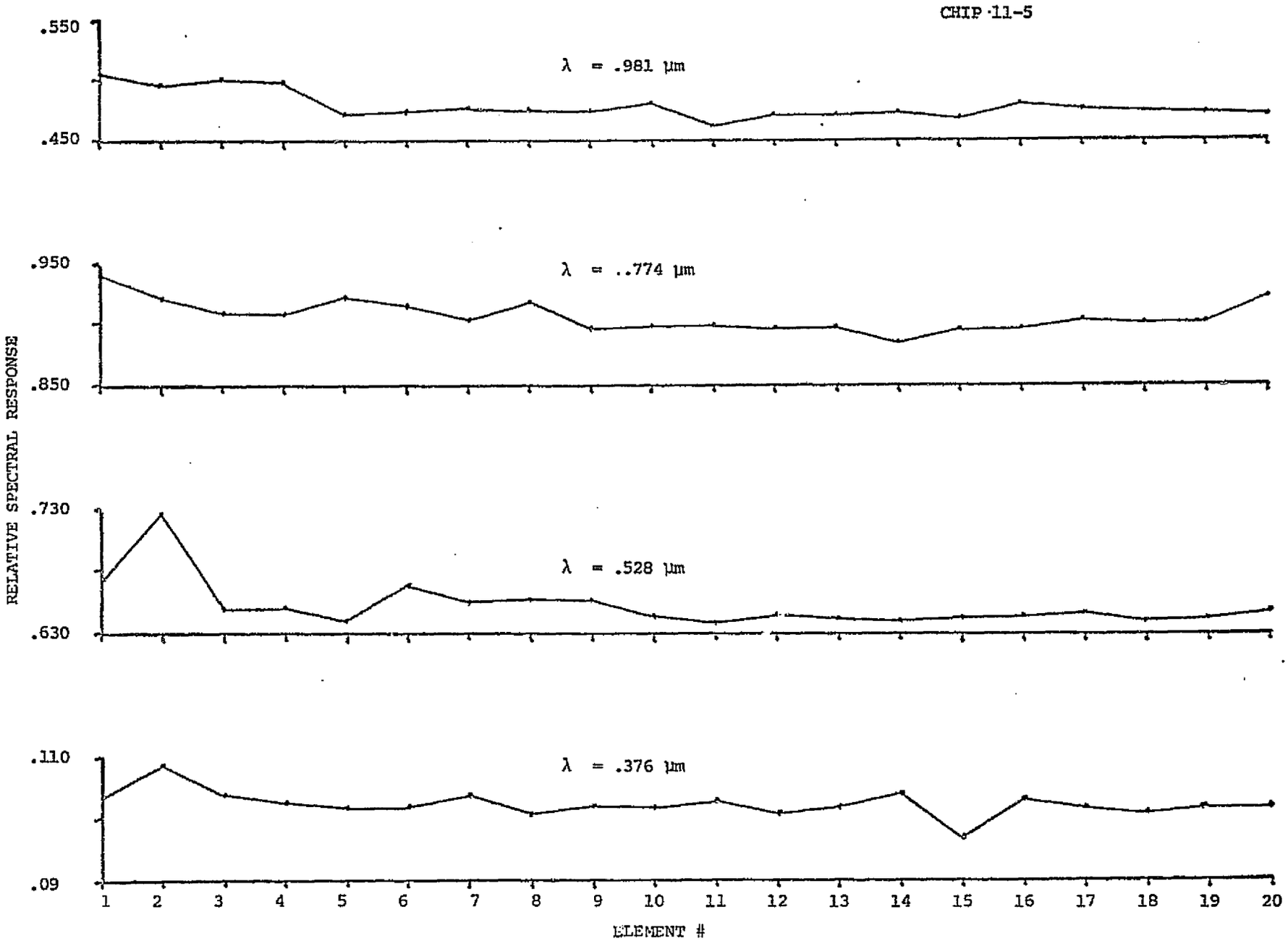
slope for a constant quantum efficiency detector with the peak shown in Figure 5-1 is 135%/μm which is 20% less than the measured value and only just within specification. The ripple has exceeded specification because the band limits happen to lie on either side of the spectral peak. The spectral curve appears quite normal with an almost constant quantum efficiency.

The quantum efficiency, η may be determined by the relation between the noise output and the irradiance. The noise-equivalent-signal exposure (NES) or the exposure at which S/N = 1 may be written:

$$NES = \left[K^2 + \frac{q H_\lambda t}{R} \right]^{1/2} \text{joule/m}^2$$

where K = constant and includes all constant noise sources

Figure 5-2. RELATIVE SPECTRA RESPONSE BY ELEMENT



q = electronic charge

H_λ = irradiance

t = integration time

$$R = \frac{q\,\eta\,\lambda A_D}{h\,c} \text{ amps/(watt/m}^2\text{) or coulombs/(joule/m}^2\text{)}$$

A_D = area of detector

h = Planck's constant = 6.625×10^{-34} joule-sec

c = speed of light = 3×10^8 m/sec

λ = wavelength

By measuring the slope of the NES^2 curve versus illumination the quantum efficiency may be found by the relationship

$$\eta = \frac{hc}{\lambda}\,\frac{1}{A_D}\,\frac{\partial(H_\lambda t)}{\partial(NES^2)}$$

A plot of NES^2 versus exposure is shown in Figure 5-3 for chip 11-5 and the quantum efficiency is found to be 70% at 650 nm.

Based on this spectral response curve it is useful to convert the irradiance requirements of the sensor at various bands into an equivalent number of electrons so that measurements taken at any spectral band may be referred to any other spectral band. The conversion shown in Table 5-4 gives the result in holes/TDI* stage to further generalize results.

*Holes describe a jargon invented by Schockley and others to describe the effective positive charge signal carrier (as opposed to the negative charged electron) in certain doped semiconductor materials.

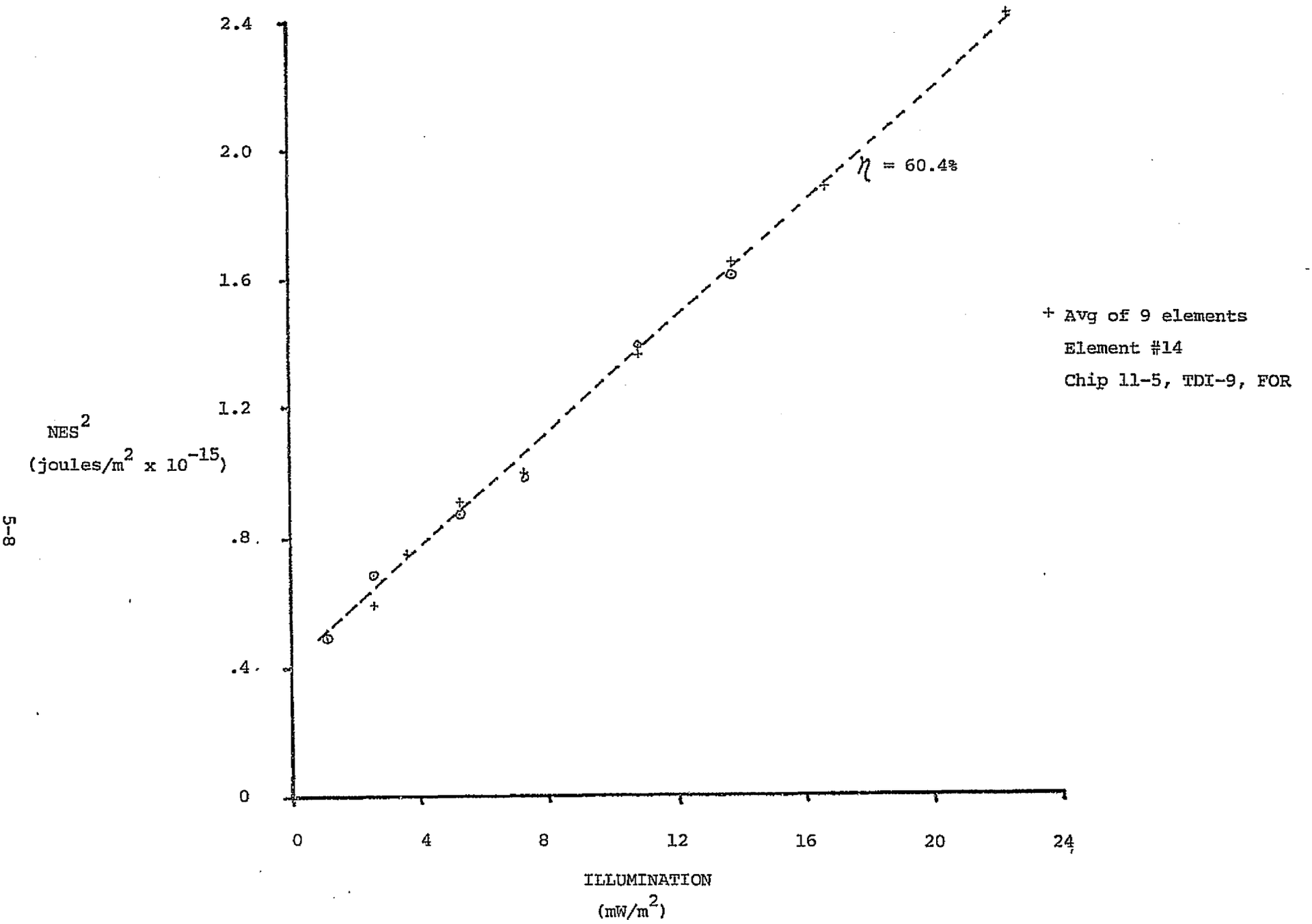


Figure 5-3. NOISE^2 VS ILLUMINATION

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TABLE 5-4

SPECTRAL BAND	CENTER WAVELENGTH	MAX IRRADIANCE W/m^2	MAX IRRADIANCE Holes/TDI Stage	SIGNAL IRRADIANCE W/m^2	SIGNAL IRRADIANCE Holes/TDI Stage
0	.485	.98	7.68×10^4	.155	1.21×10^4
1	.56	.97	8.77×10^4	.143	1.29×10^4
2	.66	.62	6.60×10^4	.087	$.93 \times 10^4$
3	.77	.41	5.1×10^4	.055	$.68 \times 10^4$
4	.855	.75	1.03×10^5	.102	1.4×10^4

TABLE 5-5

LEAKAGE DATA FOR TWO DEVICES
NUMBERS ARE IN DIGITAL COUNTS

	11-7		11-3	
EL #	FORWARD	REVERSE	FORWARD	REVERSE
1	81.6	67.6	114.1	87.4
2	110.5	97.6	96.6	575.6
3	54.8	58.0	90.2	76.5
4	92.7	82.2	351.6	361.2
5	139.8	121.3	88.9	56.2
6	165.3	153.3	87.1	72.3
7	208.2	224.9	52.5	109.9
8	174.5	165.7	31.1	104.5
9	162.0	141.0	51.5	79.6
10	124.8	108.5	128.8	139.0
11	177.7	180.3	236.2	237.2
12	110.5	100.5	91.3	92.8
13	272.7	296.5	124.3	149.6
14	134.6	161.6	139.2	189.7
15	142.4	160.0	368.4	454.8
16	414.4	435.4	107.3	200.2
17	394.5	412.4	125.4	218.4
18	676.5	638.1	156.0	262.0
19	578.3	570.3	159.3	229.5
20	333.2	327.5	237.7	266.5

$r = 98$ counts/$\mu J/m^2$ $\quad$ $r = 93$ counts/$\mu J/m^2$

$R = 1.81 \times 10^{-15}$ coulombs/μJ

5.3 Leakage

The leakage of the sensor is difficult to determine since only indirect techniques are available for its measurement. The techniques used is to compute the leakage from the change in dark level that is measured as the TDI mode changed. The change in output may be equated to leakage through the measured response of the sensor and its quantum efficiency by:

$$I_L = \frac{(X_2 - X_1) R}{(t_2 - t_1) r}$$

where X = the element output in digital counts

t = integration time

= number of TDI stages (M) x line time

R = responsivity in coulombs/$\mu J/m^2$

r = responsivity in digital counts/$\mu J/m^2$

Table 5-5 lists the difference between TDI-9 and TDI-0* for two chips tested with correlated sample readout at 79.2 μsec line times. The output changes varied between 676 counts (9.1×10^4 holes) to 37 counts (5.2×10^3 holes). This is equivalent to 356 - 20 nA/cm^2.

In an attempt to determine the leakage of the shift register the line time was increased by a factor of 2 to 158.4 μsec. The change in output should be proportional to the leakage of the output shift register. Although the changes in output were quite large in some cases the standard deviation did not change

*The TDI-0 mode results when the reverse output is being read while the array is being clocked in the TDI-9 Forward mode. In this mode no charge is being clocked into the reverse readout register, then the leakage being monitored is that of the readout register only. Simarly when the forward output is monitored and the sensor is clocked in the TDI-9 Reverse mode.

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relatively as it should. Therefore it is believed that the changes were also a function of the correlated sample thus partially masking the leakage of the output register.

5.4 Uniformity of Dark Level

The response at dark is dependent upon four factors: the bias setting of the processor itself, electrical pattern noise, the leakage of individual detectors, and the leakage of the output register and readout node. The bias of the channel sets the average level of the sensor output. Electrical pattern noise enters the output as either an offset of the average of the bus or as individual element offset differences; these are usually due to interaction of transients present in the timing and/or the video output with the processor. The leakage of individual elements contributes to farther deviation of the elements from the mean. The shift register leakage raises the average output of each bus since it contributes the same average leakage to each pixel. The performance goal for the sensor is channel-channel dark level variation of 2% of band 2 irradiance, the requirement is less than 10%. Referring to section 5.2 this equates to 6.6×10^3 holes/TDI stage to achieve 10%, and 1.32×10^3 for 2%.

Table 5-6 lists the dark level output for 4 devices measured with the correlated double sampler. Since elements 1-10 or elements 11-20 are always operated through the same channel regardless of sensor chip TDI length or direction, comparison between groups should give the chip-chip comparison if it is presumed the external amplifiers can be precisely set. For elements 1-10 the spread between chips is 251 - 523 counts or approximately 3.2×10^4 holes at TDI-0 and 5.6×10^3 within a chip. This is essentially pattern noise since no signal is entering the output register. At TDI-3 the variations increase slightly to 4.1×10^4 holes spread between chips and 1.3×10^4 holes within a chip.

The spread within a chip meets the 10% of maximum band 2 requirement but not the 2% goal.

There is a large spread of dark levels between groups 1-10 and 11-20. It is suspected that this is due to a large leakage in the output register of group 11-20 that is related to register design. This has been confirmed by visual observation of the unprocessed video waveform on several devices. However, no cause for this preferential leakage has yet been located.

TABLE 5-6

DIFFERENCE IN CHANNEL-TO-CHANNEL OUTPUT AT DARK

		TDI-0				TDI-3			
	CHANNEL	FOR		REV		FOR		REV	
CHIP	NO.	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
11-3	1-10	394	381	338	323	464	395	386	355
	11-20	1323	1192	1862	1837	1394	1304	2112	1891
11-7	1-10	293	251	378	373	383	272	444	391
	11-20	2119	1904	978	972	2297	1981	1173	1032
11-17	1-10	523	476	342	337	615	508	441	360
	11-20	2073	1886	1830	1820	2154	1933	2009	1860
11-4	1-10	300	284	259	254	387	318	1657*	274
	11-20	631	602	1091	1084	744	671	1201	1131

where 1 count $\cong$ 120 electrons

* one leaky element

The measured offset for a chip operated by the high speed sampler in the TDI-9 mode is shown in the table below. In these measurements the bias for each

		TDI-9			
		FOR		REV	
CHIP		MAX	MIN	MAX	MIN
11-17	1-10	939	780	966	673
	11-20	852	380	892	450

where 1 count $\cong$ 550 electrons

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channel was not necessarily the same for a group of elements forward and reverse. The specification of 10% variation here requires 75 counts maximum difference between elements and this specification was not met. The largest contributor to the very large variation among elements was feed-thru noise (electrical transients). This was obvious in visual observations of the video waveform from the sensor. Where transients occur in the line time due to sensor phase transitions, large offsets occur in the time frame of each element.

5.5 Signal-Noise Ratio

The predicted signal-to-noise performance for the two methods by which the sensor was measured are shown in Table 5-7. The table shows that both techniques are expected to exceed requirements with comfortable margins. With the correlated double sample readout techniques the predicted margin is 176% for TDI-9 in the worst band (band 3). For the simple video sample technique the predicted margin is 100%. The difference between these two techniques is not great because at TDI-9 for the specified irradiances the noise is being dominated by signal shot noise according to the model.

Table 5-8 shows the measured signal to noise performance of sensor 11-5 for its three different TDI modes in the forward direction. The measurements were made at 13.07 mW/m^2 in the TDI-3 and TDI-6 modes and 15.7 mW/m^2 for TDI-9. The values in parentheses are extrapolations to 15.7 mW/m^2. Since the measurement was taken at 79.1 μsec using band limited 400 - 800 nm 6000^{o}K blackbody radiation, these measurements can be viewed as being at the equivalent signal level of band 1 (assume all energy centered at the mean wavelength $\sim$600 nm). Under this assumption the specification is exceeded at TDI-6 and TDI-9. In TDI-9 the margin is about 20% less than calculated in the noise model for the high speed sampler.

TABLE 5-7. NOISE ANALYSIS OF TDI-CHIP

	SPECTRAL BAND (nm)	IRRADIANCE AT DETECTOR: IRRADIANCE @ 8.0 µsec (W/m^2)	IRRADIANCE AT DETECTOR: ELECTRONS	PREDICTED S/N: HIGH SPEED SAMPLER	PREDICTED S/N: PHOTON NOISE LIMIT	PREDICTED S/N: CORRELATED DOUBLE SAMPLE
0	450 - 520	.155	1.18×10^5	178 - 296	344	333
1	520 - 600	.143	1.16×10^5	279 - 307	340	330
2	630 - 690	.087	$.83 \times 10^5$	222 - 251	288	275
3	740 - 800	.055	$.62 \times 10^5$	178 - 207	249	235
4	800 - 910	.102	1.27×10^5	294 - 323	356	346

M = 9 stages N = 10 channels/electrometer Pixel Size = 76 µm x 76 µm

TABLE 5-8. MEASURED BAND 1 S/N RATIO OF CHIP 11-5

REQUIRED PERFORMANCE FOR BAND 1 -- SNR = 145

EL #	TDI-3 @ 13.07 mW/m^2	TDI-6 @ 13.07 mW/m^2	TDI-9 @ 15.7 mW/m^2
1	111(128)	197(227)	278
2	102(118)	198(228)	281
3	110(127)	193(223)	272
4	110(127)	185(213)	276
5	79(91)	159(183)	160
6	102(118)	198(228)	248
7	114(132)	190(219)	277
8	107(123)	195(225)	288
9	103(119)	185(213)	286
10	121(140)	193(223)	273
11	119(137)	210(242)	287
12	113(130)	228(263)	287
13	134(155)	224(258)	306
14	136(157)	196(226)	300
15	129(149)	145(167)	169
16	128(148)	224(258)	301
17	121(140)	220(254)	304
18	134(155)	209(241)	288
19	120(138)	195(225)	293
20	163(188)	267(308)	415

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Table 5-9 lists the signal-to-noise ratio of chip 11-17 measured at the 8 μsec line time at 70 mW/m^2 illumination at 650 nm. The values range from 30.2 to 55.3, which is only 15 - 25% of the predicted value. Here the noise appears to increase very rapidly with increasing exposure and is thought to be related to the still not completely proven test stand.

TABLE 5-9. SENSOR 11-17 S/N

TDI-9, For H = 70 mW/m^2

EL #	S/N
1	39.44
2	43.46
3	46.10
4	32.21
5	46.44
6	42.00
7	52.80
8	55.32
9	48.28
10	47.31
11	39.15
12	49.82
13	54.21
14	30.24
15	55.61
16	52.41
17	52.92
18	40.54
19	32.84
20	50.50

The measured performance of these devices in the CDS exerciser has also differed from predicted values by significant amounts, but the identified problem is a high level of dark noise. In an attempt to locate the source of the excess noise it is useful to review briefly the noise model. The general noise model may be written:

$$\overline{Q}_n = \left[\left(\begin{matrix}\text{signal}\\ \text{shot}\\ \text{noise}\end{matrix}\right)^2 + \left(\begin{matrix}\text{CCD}\\ \text{trapping}\\ \text{\& release}\\ \text{noise}\end{matrix}\right)^2 + \left(\begin{matrix}\text{sensor}\\ \text{leakage}\\ \text{shot}\\ \text{noise}\end{matrix}\right)^2 + \left(\begin{matrix}\text{diode}\\ \text{reset}\\ \text{noise}\end{matrix}\right)^2 + \left(\begin{matrix}\text{on chip}\\ \text{amplifier}\\ \text{noise}\end{matrix}\right)^2 + \left(\begin{matrix}\text{off chip}\\ \text{amplifier}\\ \text{noise}\end{matrix}\right)^2 + \left(\begin{matrix}\text{quantizing}\\ \text{noise}\end{matrix}\right)^2 \right]^{1/2}$$

With correlated double sampling the model is reduced by the elimination of the reset noise. Expressing the model algebraically, where all terms in the bracket have the units of noise charge squared referred to the input of the first on chip amplifier yields the following result.

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CCD-TDI NOISE MODEL

$$Q_n = \frac{1}{q}\left[qRE + q^2 M_C PN_t \frac{M_S}{N_D}\left(1 - e^{-\frac{t}{Pt_e}}\right)e^{-\frac{t}{Pt_e}} + q(m+1)I\,t + kTC_S + \varepsilon_{n1}{}^2 \Delta f_{n1} C_S{}^2 + \frac{I_{n2}{}^2 \Delta f_{n2} C_S{}^2}{g_m{}^2} + \left(\frac{1/\sqrt{12}\; C_S}{1024 G g_m R_E}\right)^2\right]^{1/2} \text{ holes,}$$

with typical values:

$$= \frac{1}{1.6\times10^{-19}}\left[2.56\times10^{-34}E + 1.16\times10^{-39} + 1.5\times10^{-34} + 7.2\times10^{-34} + 8.8\times10^{-36} + 3.6\times10^{-36} + 1.50\times10^{-35}\right]^{1/2}$$

which at dark is:

$$= \frac{1}{1.6\times10^{-19}}\left[8.97\times10^{-34}\right]^{1/2} = 187 \text{ holes}$$

With correlated double sampling this becomes:

$$Q_n = \frac{1}{1.6\times10^{-19}}\left[1.77\times10^{-34}\right] = 83 \text{ holes}$$

Assumes: $I_L = 3.0$ pA $\qquad \varepsilon_{n1} = 15$ nV/Hz$^{1/2}$

$C_S = .18$ pf $\qquad$ Integration time = 234 μsec

TDI = 3 $\qquad G = 7$

These values are substantially lower than the measured values. Other noise sources could include leakage in the output register and collection diode, which was not included in this model. To measure output register leakage, the clock frequency was halved to double the time to collect leakage charge in the

output register and the signal and response standard deviation were compared with those measured at 78 μsec per line, both with TDI-0. Data was taken only with the CDS exerciser. Results for chip 11-17, while not consistent, indicate leakage for elements 1 through 10 were 97 pA and 68 pA respectively from response and standard deviation changes, which would predict NES = 18 to 22 nJ/m^2, approximately the measured value on this chip. For elements 11 through 20, the leakage values are 374 and 1290 pA, corresponding to NES of 43 and 80 nJ/m^2, which span the measured value of about 60 nJ/m^2.

Thus the source of excess noise in these sample chips at the slower rate of the CDS equipment appears to be leakage either in the output register, or in the summing gate and collection diode, or some effect in the signal processor. The consistent difference between the first and second output registers on each side of the chip suggests that the effect, if it originates on chip, is not bulk leakage in the silicon, but rather current flow along an unwanted inversion path near the output diode or some other unintended detail in the mask design. There was unfortunately insufficient time to isolate and in addition correct this problem during phase II. Experience on similar devices in these laboratories, indicates that the correction should be straight forward. The effect is far less serious when the chips are operated at the higher data rates intended for the application.

5.6 Dynamic Range

The relative output versus illumination is shown in Figure 5-4 for chip 11-5 for the three TDI modes*. The output is linear to the extremes of

*In this section all irradiances are with respect to a 5500K source band limited to 0.4 μm to 0.8 μm.

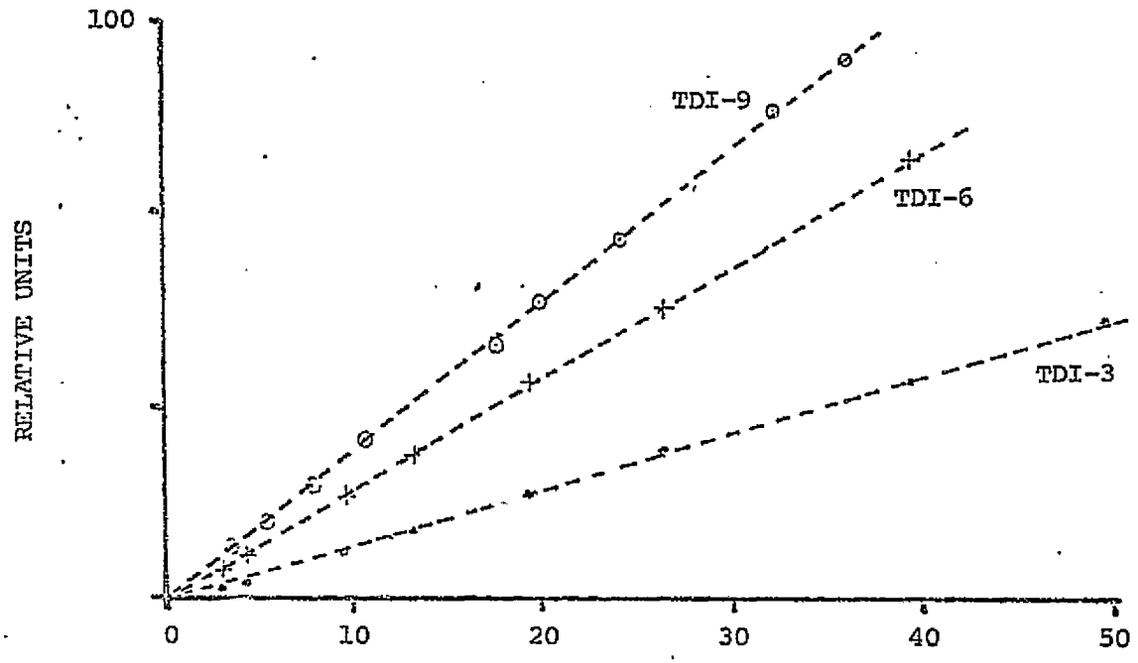

Figure 5-4. TDI SENSOR GAIN

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the measurement. Because of the 10x slower speed of operation these measurements indicate that the device would be linear to beyond 350 mW/m^2 at TDI-9 and a line rate of 8 μsec and beyond 500 mW/m^2 for TDI-3. These measurements were limited by the dynamic range of the A/D converter, not the sensor chip.

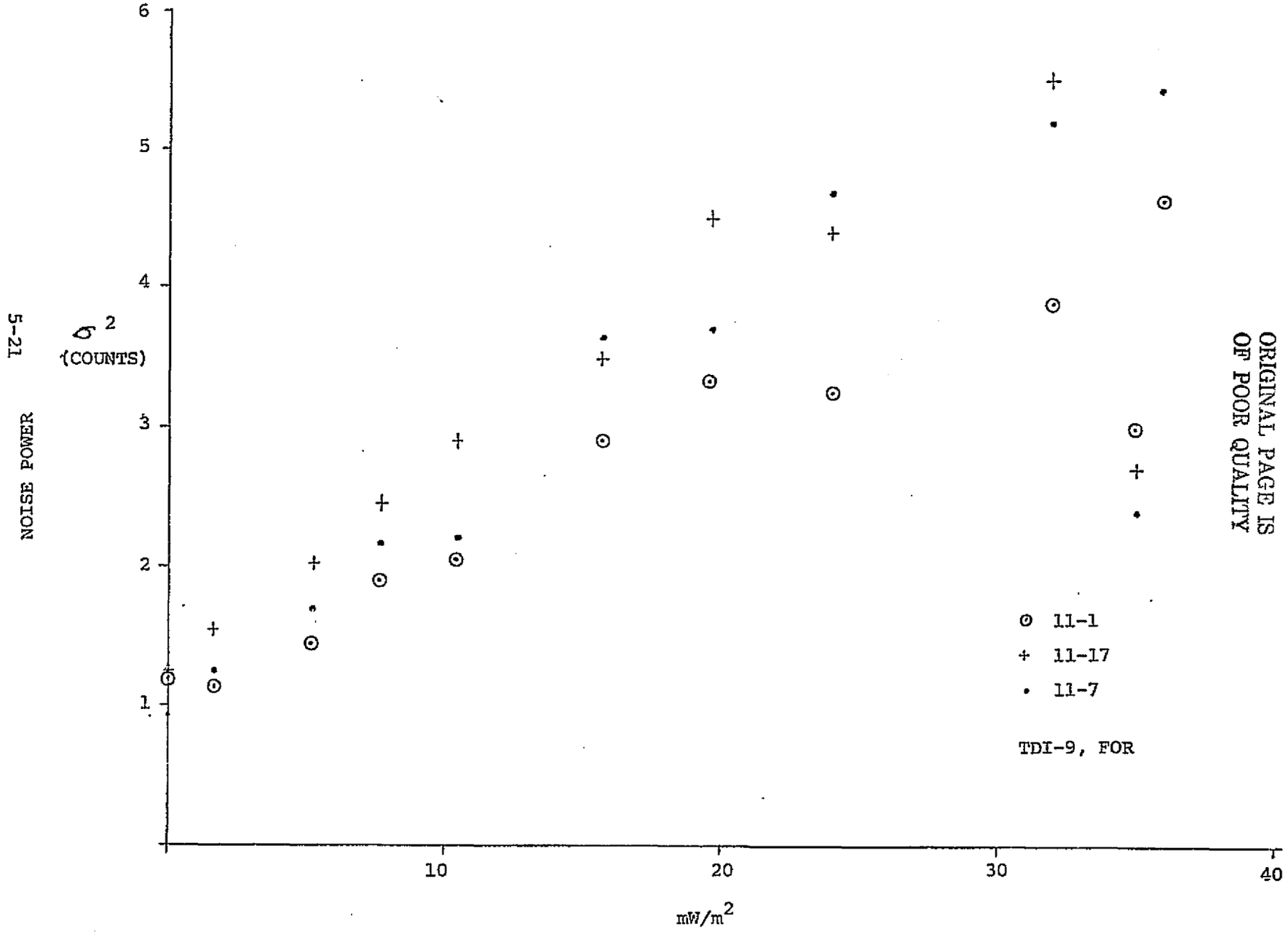
The linear dynamic range of an element in the array does not however tell the whole story of dynamic range. Plots of noise power versus exposure, like those used to calculate quantum efficiency, have shown a nonlinearity at higher exposure contrary to theory. A plot standard deviation squared versus illumination is shown in Figure 5-5. These nonlinearities occur despite linear signal output. It is theorized that the nonlinearity is due to a saturation occurring in the along scan (X) direction that manifests itself as a smearing of adjacent pixels. This smearing would thus cause sample to sample correlation, and thus, reduce noise. Since it occurs in the along scan (X) direction no flat field measurement would show it. Further evaluation is necessary to determine if these nonlinearities are due to true saturation or to test errors, and to measure effects on other parameters such as MTF.

5.7 Linearity and Gain

Figure 5-6 is a plot of the deviation from a straight line between dark and the output at 90 mW/m^2 for several elements chip 11-5 at TDI-3. The deviation from the straight line is due to (1) calibration error of the individual light levels, and (2) the nonlinearities of the sensor itself. The figure is plotted in A/D counts, when the maximum signal is approximately 2200 counts. This plot shows a deviation of less than 1% of maximum signal.

The deviation from the straight line by element at 13 mW/m^2 is plotted in Figure 5-7. The output level is approximately 350 counts. The spread among these elements if 4.6% of this new maximum signal output.

Figure 5-5. NOISE VERSUS ILLUMINATION



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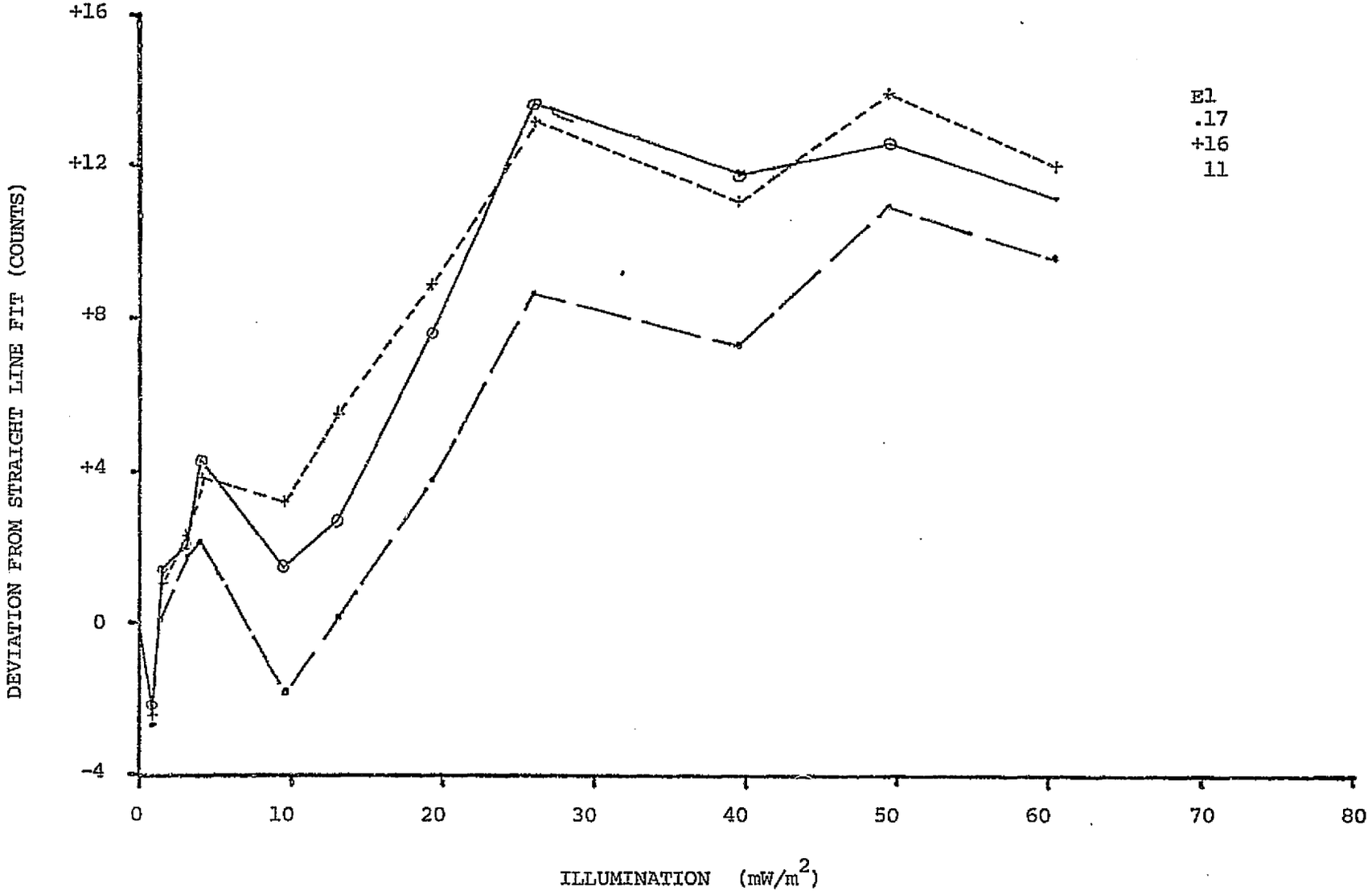
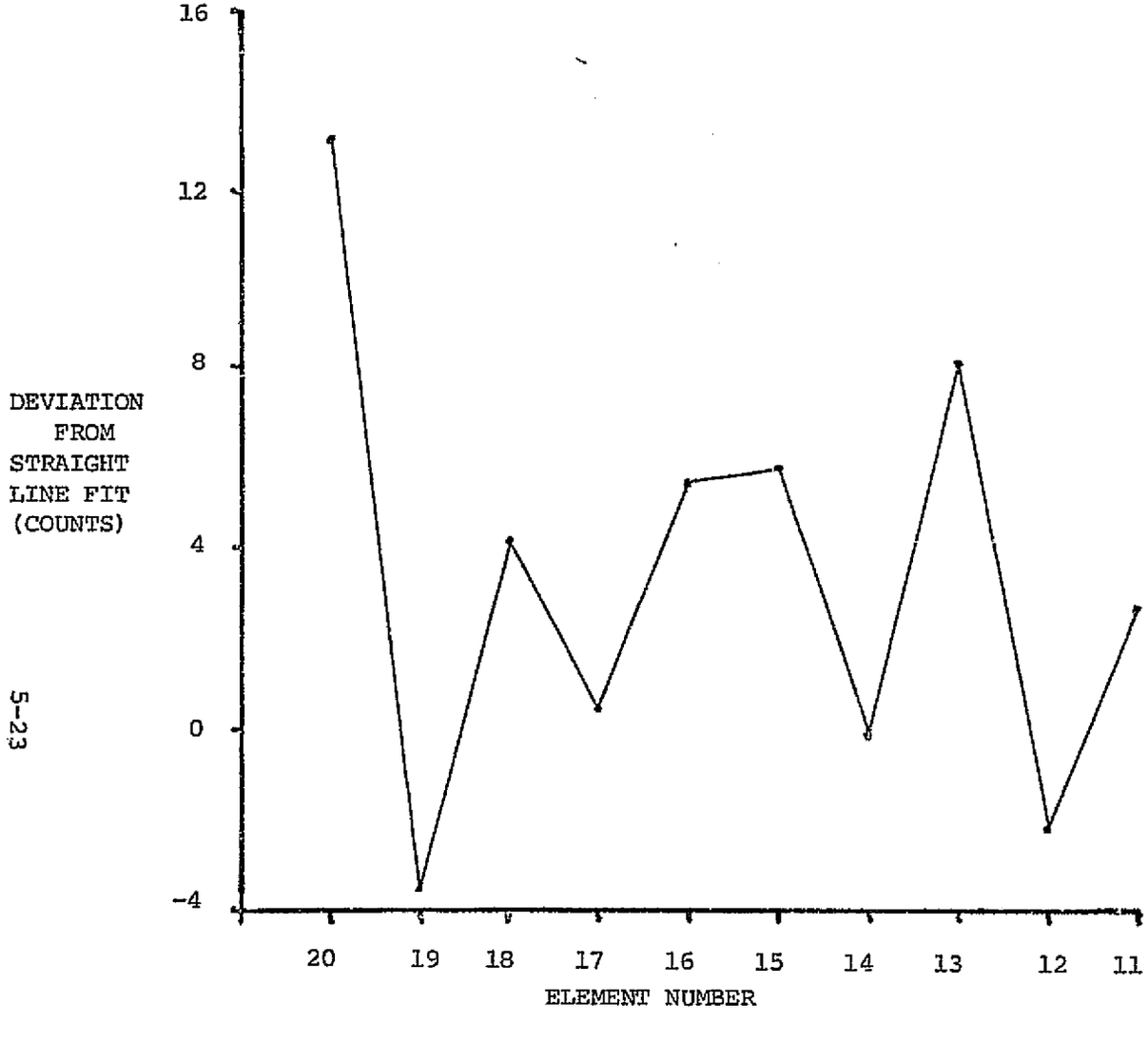


Figure 5-6. DEVIATION FROM STRAIGHT LINE FITTED BETWEEN DARK AND MAXIMUM OUTPUT



H_λ = 13.06 mW/m^2

TDI-9 ,FOR

Figure 5-7. DEVIATION VS ELEMENT

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The gain variation among chips is illustrated by Table 5-10 which shows the gains for two chips normalized to the maximum gain at TDI-9 and 15.7 mW/m^2. The maximum gain variation is 10% for the two chips. In addition, the chip-to-chip gain was within 10%. This is unusually close since the gain of the chip is primarily controlled by the output FET transconductance, which can vary as much as 2:1 between chips.

TABLE 5-10

Normalized Gain H = 15 mW/m^2 TDI-9, For

EL #	CHIP 11-17	CHIP 11-7
1	.94	.90
2	.91	.95
3	.96	.94
4	.98	.97
5	.99	.97
6	.99	.98
7	.99	.99
8	.98	1.00
9	1.00	.99
10	.99	.97

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APPENDIX A

TIME DELAY AND INTEGRATION IMAGE SENSORS

1.0 INTRODUCTION

In certain applications, it is important to view the object plane from a platform which has linear motion relative to the object plane. In such circumstances, the object/sensor motion may be used to generate one dimension of the image field. A typical example of this type of image generation is the remode sensing platform of the Landsat program. This mode of image generation is commonly called the "pushbroom" mode. Figure 1 shows a schematic diagram of an electro-optical system using a linear array of sensor elements in the "pushbroom" mode. As the sensor array moves across the scene due to the relative motion, the scene is synthesized into a series of strips. If a linear array is used, then there is a tradeoff between signal-to-noise ratio and resolution in the along-track direction. The use of CCD's in the TDI mode has allowed the "pushbroom" concept to be extended to provide additional sensitivity (signal) without a sacrifice in resolution.

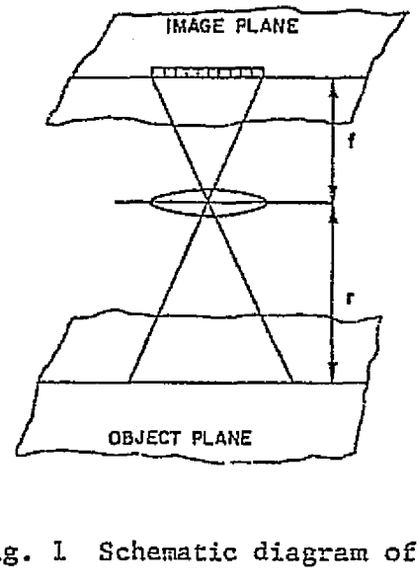

Fig. 1 Schematic diagram of an imaging system.

2.0 THE PUSHBROOM IMAGING MODE

When the sensor and the scene to be viewed have a constant relative velocity, a linear array of sensor elements can be used for imaging as shown in Fig. 2. The minimum geometrically resolvable dimension in the along-track direction in the object plane, d_{geom}, is determined by the speed of the sensor projected onto the object plane via the optical system, V_o, and the integration time of the sensor, T; i.e.,

$$d_{geom} = V_o T \quad , \tag{1}$$

where d_{geom} is the along-track distance covered by a sensor element projected onto the object plane in an integration time. Using the magnification relation, the speed of a point in the object plane projected onto the image plane, V_i, is

$$V_i = (f/r)\, V_o \quad , \tag{2}$$

where f = focal length of the optical system.
r = object plane to image plane distance.
V_o = speed of a point in the image plane projected onto the object plane.

The output signal is proportional to the input irradiance, H, and

the integration time; i.e.,

$$S \alpha HT \quad . \qquad (3)$$

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Therefore, the ratio of the geometrical resolution and the signal out of the array is independent of T. This represents a basic tradeoff for the pushbroom mode; i.e., T can be reduced to decrease d_{geom}, but S also decreases. Another factor is the data rate changes when the exposure time is altered.

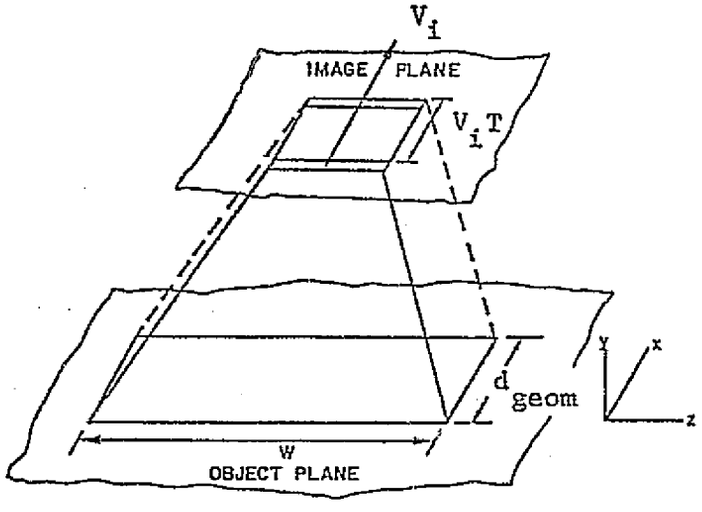

Fig. 2 Pushbroom imaging concept (optics not shown).

3.0 THE TIME DELAY AND INTEGRATION (TDI) MODE

If the image plane were composed of a number (M) of elements contiguous in the x-direction to form an array of columns, if the columns were electrically delayed in the x-direction at the same speed, V_i, as the scene is scanned across the image plane, and if the outputs from all elements in a given column were added, then the output signal would be M times larger than that from a single line array of equal elemental dimensions. This situation is shown in Fig. 3 and is called the time delay and integration mode. Other names are delay-and-add and image-motion compensation modes. The basic result is that the signal in Eq. (3) is increased by the factor M while geometrical resolution in Eq. (1) is unchanged. Thus, the new equations analogous to Eqs. (1) and (3) are

$$d_{geom} = V_o T \ , \qquad (4)$$

and

$$S \alpha HMT . \qquad (5)$$

A major advantage of the TDI mode is that the exposure time is increased by the factor M without affecting the geometrical resolution. This improves the low-light-level capability without affecting the resolution or data rate. An advantage is the electrically alterable exposure time without a change in the output data rate.

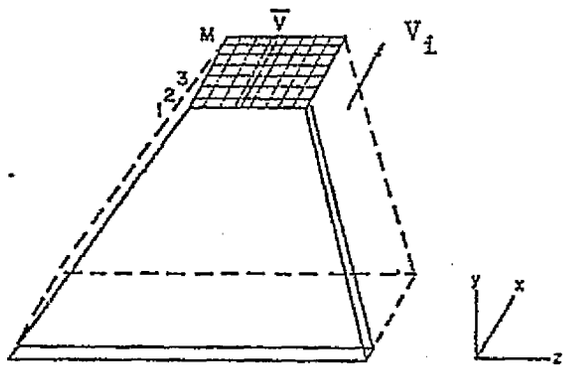

Fig. 3 Time delay and integration (TDI) concept (optics not shown).

4.0 TDI ARRAY ORGANIZATION

The natural TDI CCD chip organization, shown in Fig. 4, is basically a parallel-serial design. The parallel imaging columns are composed of M delay-and-add stages (CCD stages). These N columns are multiplexed into an N-stage CCD serial shift register for readout. There is no need for separate frame or line storage with this mode of operation; i.e., all of the columns are optically active. Only the horizontal output register is shielded from light.

5.0 NOISE LIMITED RESOLUTION

For low-light levels, the TDI imager would operate in the noise limited regions; i.e., the minimum resolvable dimension in the along-track direction is given by

$$d_{min} = V_o T \left[\frac{CSAMHT/e}{(SAMHT/e + MN_1^2 + N_2^2)^{\frac{1}{2}}} \right]^{-1} \qquad (6)$$

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where

C = scene constrast,
S = responsivity in mA/watt,
A = optically active area of sensor row,
M = number of TDI stages,
T = integration time,
H = irradiance on the image plane,
e = electronic charge,
N_1 = noise (in number of electrons) introduced at each TDI stage, and
N_2 = noise (in number of electrons) introduced by the output amplifier [1].

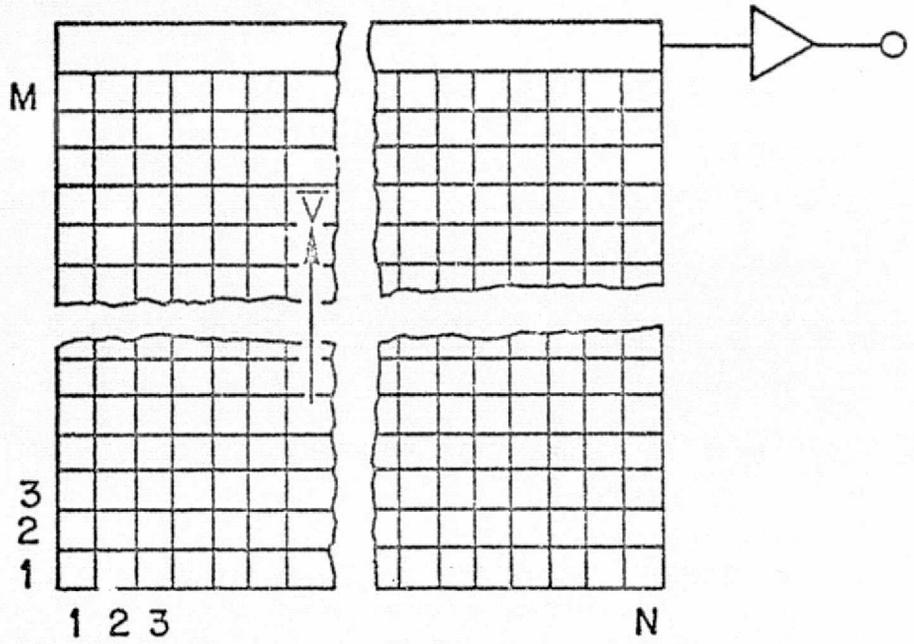

Fig. 4 Time delay and integration array organization.

There are three cases to be examined with regard to the functional dependence of d_{min} on M: (1) if photon noise dominates, then d_{min} is proportional to $M^{-\frac{1}{2}}$; (2) if N_1 dominates, the d_{min} is proportional to $M^{-\frac{1}{2}}$; and (3) if N_2 dominates, then d_{min} is proportional to M^{-1}.

6.0 SPATIAL FREQUENCY RESPONSE

In any approach to low-light-level imaging it is necessary to be able to predict, by the use of appropriate theory, the ability of the system to resolve detail. In low-light-level imaging the

maximum quantity of information transmitted is frequently not of great interest, and it is often necessary to give up information of a certain type in order to increase the quantity of information of other types. However, in order to make comparisons it is necessary to know the relationships of the image transfer properties of individual system components to the equivalent property of the complete system. In addition, it is necessary to know how well each component transfers image details and contrasts.

Use of the modulation transfer function (MTF) makes it possible to compute the effects on image rendition of the different elements through which an image is transmitted between the scene and the observer. Actually the information continues on to the observer's brain, and some consideration as to what is required to recognize an object is necessary. Any mechanism that operates on or collects information modifies it in some way, so that information delivered in hard-copy form is different from the original scene information. These differences can be predicted to a great extent by the use of MTF's. Manipulation of the MTF's permits the description of the difference between the input information and the output information without an exact knowledge of the nature of the information itself. Because the effects of each element that transmits the information can be accounted for separately and the total effect determined by the multiplication of each of these functions, their use is extremely advantageous. The close relationship between spatial frequency and fineness of detail, which preserves intuitive clarity, makes the MTF a powerful tool in the analysis of imaging systems.

The effects which cause the imaging array response (signal) to decrease at high spatial frequencies are: (1) the geometry of the integration aperture, (2) the degree to which the average speed of the charge packets is matched to the speed of the scene moving across the array, (3) the discrete nature of the charge motion, and (4) the charge transfer inefficiency. These effects are treated separately in the remainder of this section. Since any scene can be analyzed into Fourier components in object space (x,y), a general treatment of the response of a sensor array reduces to an analysis of the response to a sinusoid of arbitrary spatial frequency.

6.1 Integration MTF (Geometry of Integration Aperture)

If the distance between samples on the image plane in the x-direction is p, then the Nyquist frequency is

$$f_n = 1/2p \quad . \qquad (7)$$

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The Fourier component of the irradiance on the array at spatial frequency f is

$$H_1 = H_0 \left[1 + m \cos (2 \pi f x) \right] . \tag{8}$$

This can also be written

$$H_1 = H_0 \left[1 + m \cos \left(\pi \frac{f}{f_n} \frac{x}{p} \right) \right] . \tag{9}$$

If the integration aperture is Δx in width, then the output charge pattern is that due to a different intensity pattern H_2

$$H_2 = \frac{1}{p} \int_{x_i - \frac{1}{2}\Delta x}^{x_i + \frac{1}{2}\Delta x} H_0 \left[1 + m \cos \left(\pi \frac{f}{f_n} \frac{x}{p} \right) \right] dx \tag{10}$$

(10)

Integrating Eq. (1) and simplifying gives

$$H_2 = \frac{H_0}{p} \left[1 + m \frac{\sin \left(\frac{\pi}{2} \frac{f}{f_n} \frac{\Delta x}{p} \right)}{\frac{\pi}{2} \frac{f}{f_n} \frac{\Delta x}{p}} \cos \left(\pi \frac{f}{f_n} \frac{x}{p} \right) \right] . \tag{11}$$

Therefore, the MTF of the integration process is

$$MTF_{integ} = \frac{\sin \left(\frac{\pi}{2} \frac{f}{f_n} \frac{\Delta x}{p} \right)}{\frac{\pi}{2} \frac{f}{f_n} \frac{\Delta x}{p}} \tag{12}$$

In the TDI CCD array organization, the integration aperture Δx is equal to the distance between samples, p, (this is also true in the y-direction). Therefore, the picture elements are contiguous in both directions. This is shown in Fig. 5 for a 3-phase system. Then Eq. (12) reduces to

$$MTF_{integ} = \frac{\sin \left(\frac{\pi}{2} \frac{f}{f_n} \right)}{\frac{\pi}{2} \frac{f}{f_n}} . \tag{13}$$

The integration MTF in the z-direction will be given by the same expression with the appropriate modification if p_z is different from p_x.

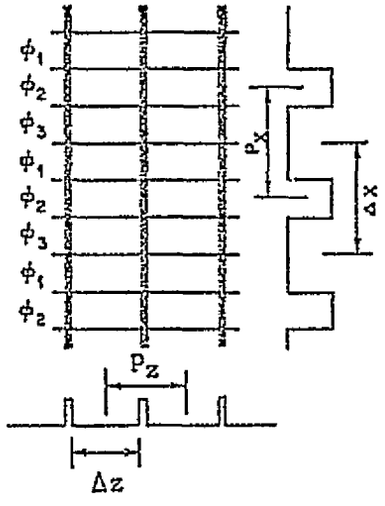

Fig. 5 Schematic diagram showing integration aperture dimensions.

6.2 Synchronism MTF (Matching Electrical and Mechanical Scans)

If the average speed of the charge packets is not exactly equal to the speed of the motion of the scene across the image plane, then the response will be degraded [2]. If the difference between the average speed of the charge packets ($\bar{V}$) and the speed of the scene on the image plane (V_i) is ΔV, then after M TDI stages the charge packets will be displaced from where they should be if the synchronism were perfect, by the distance $MP(\Delta V/V)$. In effect the array sees a traveling wave instead of a fixed Fourier component representing each spatial frequency. The MTF degradation due to this effect can be determined by noting the equivalence between (1) an infinitesimal aperture sampling a traveling wave with relative speed ΔV for a time MP/V and (2) an aperture of width $MP(\Delta V/V)$ sampling a stationary wave as shown in Fig. 6. Therefore the form of this MTF is Eq. (13) with Δx replaced by $MP(\Delta V/V)$ i.e.,

$$(MTF)_{\Delta V} = \frac{\sin\left(\frac{\pi}{2}\,\frac{f}{f_n}\,M\,\frac{\Delta V}{V}\right)}{\frac{\pi}{2}\,\frac{f}{f_n}\,M\,\frac{\Delta V}{V}} \quad . \tag{14}$$

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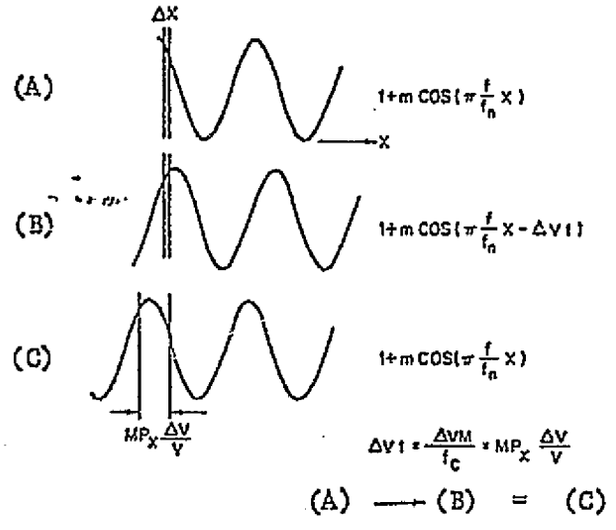

Fig. 6 Diagrams indicating the effect of non-synchronism on aperture size.

Figure 7 shows curves of $(MTF)_{\Delta V}$ vs. f/f_n with $M(\Delta V/V)$ as the parameter. For $M(\Delta V/V) = 2$, the MTF is 0.64 at $f/f_n = \frac{1}{2}$ and zero at $f/f_n = 1$. Further MTF degradation due to higher $M(\Delta V/V)$ would be intolerable. This is an important design criterion for TDI CCD arrays. If it is assumed that a practical value of $\Delta V/V$ is 1%, then using the criterion that $M(\Delta V/V) \leq 2$, gives $M \leq 200$. Therefore for $\Delta V/V \simeq 1\%$, more than 200 delay-and-add stages is impractical. The inequality $M(\Delta V/V) \leq 2$ is the primary criterion used to choose the number of TDI stages.

6.3 Discrete charge motion MTF

Even if the average speed of the charge packets is equal to the speed at which the image moves across the sensors, there will still be a loss of response due to the discrete nature of the charge transfer compared with the uniform motion of the scene across the sensor [3]. Between two successive transfers of charge, the image will move a distance $d = p/n_\phi$, where p is the center-to-center spacing between CCD stages (not electrodes) and n_ϕ is the number of transfers per stage (number of phases). This motion will change the sensitivity function for an element in the direction of motion from $S_1(x)$ to $S_2(x)$ where

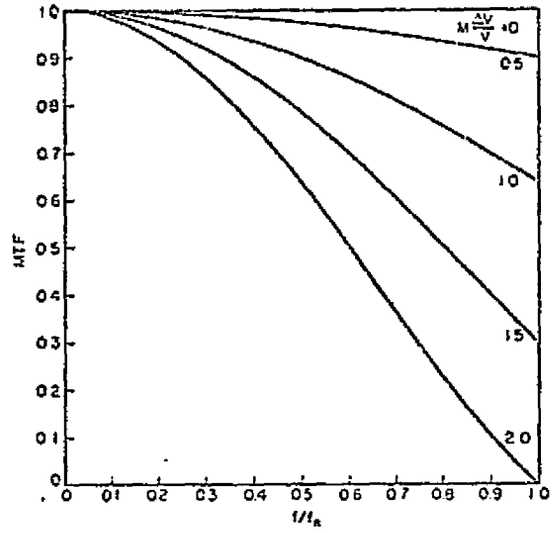

Fig. 7 MTF due to non-synchronism versus spatial frequency.

$$S_2(x) = \frac{1}{d}\int_{d/2}^{d/2} S_1(x-x')\,dx' \quad . \tag{15}$$

The response will thus be changed from

$$R_1(f) = \int_{-\infty}^{\infty} S_1(x)e^{i2\pi fx}dx \tag{16}$$

to

$$R_2(f) = \int_{-\infty}^{\infty} S_2(x)e^{i2\pi fx}dx \quad . \tag{17}$$

Substituting Eq. (15) into Eq. (17) gives

$$R_2(f) = \frac{1}{d}\int_{-\infty}^{\infty}\left(\int_{-d/2}^{d/2} S_1(x-x')\,dx'\right) e^{i2\pi fx}dx \quad . \tag{18}$$

Making the substitution w = x-x' gives

$$R_2(f) = \frac{1}{d}\int_{-d/2}^{d/2}\left(\int_{-\infty}^{\infty} S_1(w)e^{i2\pi fw}dw\right)e^{i2\pi fx'}\,dx'$$

$$= \frac{1}{d}\int_{-d/2}^{d/2} R_1(f)e^{i2\pi fx'}\,dx'$$

$$= R_1(f)\,\frac{\sin(\pi fd)}{\pi fd} \qquad (19)$$

Using $f_n = 1/2p$ and $d = p/n_\phi$ in Eq. (19), and recognizing that the sin(x)/x factor as the MTF due to the discrete nature of the charge transfer gives

$$MTF_{disc.} = \frac{\sin\left(\frac{\pi}{2}\,\frac{f}{f_n}\,\frac{1}{n_\phi}\right)}{\frac{\pi}{2}\,\frac{f}{f_n}\,\frac{1}{n_\phi}} \quad . \qquad (20)$$

At the Nyquist frequency the MTF is

0.900 for $n_\phi = 2$,
0.955 for $n_\phi = 3$,
and 0.974 for $n_\phi = 4$.

Therefore a four-phase device gives the highest MTF. This is because the charge motion is more nearly continuous.

6.4 Transfer inefficiency MTF

The gain and phase shift due to transfer inefficiency are [3]

$$G_n = \exp\left[-n\varepsilon\,(1-\cos 2\pi fp)\right] , \qquad (21)$$

and

$$\Delta\phi_n = n\varepsilon \sin(2\pi fp) \quad , \qquad (22)$$

where n is the number of transfers and ϵ is the charge transfer inefficiency. Eq. (22) is the transfer MTF in arrays having separate integration and transfer; however, it does not apply to the x-direction of TDI imagers. This is because charge packets added at different points along the columns see different numbers of transfers and different phase shifts. For the x-direction of a TDI imager, the transfer MTF can be determined by computing the output signal resulting from a sinusoidal irradiance function of spatial frequency f; i.e.,

$$H_1(x) = H_o \ (1 + m \sin 2\pi fx) \quad . \tag{23}$$

After N transfers during which the image is moved down the array, the output charge pattern will be that due to a different intensity pattern $H_2(x)$:

$$H_2(x) = \frac{1}{N} \sum_{n=1}^{N} H_o \left[1 + n\, G_n \sin\left(2\pi fx + \Delta\phi_n\right)\right] \quad , \tag{24}$$

where G_n and $\Delta\phi_n$ are given by Eqs. (21) and (22). The cumulative transfer MTF is given by the ratio of the output modulation to input modulation. Expanding Eq. (24), using the approximation

$$\sum_{n=1}^{N} g(n) \simeq \int_{0}^{N} g(n)\, dn \quad , \tag{25}$$

and manipulating gives:

$$(MTF)_{\epsilon,x} = \frac{1}{N(a^2 + b^2)} \left(\left\{ a - \exp(-Na) \left[a \cos(Nb) - b \sin(Nb) \right] \right\}^2 + \left\{ b - \exp(-Na) \left[a \sin(Nb) + b \cos(Nb) \right] \right\}^2 \right)^{\frac{1}{2}} \tag{26}$$

where

$$a = \epsilon \left[1 - \cos\left(\pi f / f_n\right)\right] \quad \text{and}$$

$$b = \epsilon \sin\left(\pi f / f_n\right) \quad .$$

Consider, for example, a 100 stage TDI imager using four-phase clocking and having n = 400 and $\epsilon = 10^{-4}$. Then at the Nyquist

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limit, $(MTF)_{\varepsilon,x} = 0.961$.

Transfer in the horizontal direction (2) is not accompanied by TDI in that direction; therefore, the $(MTF)_{\varepsilon,z}$ is given by Eq. (21).

In summary, the MTF in the direction of TDI is the product:

$$(MTF)_x = (MTF)_{integ,x} \times (MTF)_{\Delta V} \times (MTF)_{disc.} \times (MTF)_{\varepsilon,x} \quad . \tag{27}$$

The MTF in the horizontal direction is the product:

$$(MTF)_z = (MTF)_{integ,z} \times G_n \quad . \tag{28}$$

7.0 REFERENCES

1. S. B. Campana, "Charge-Coupled Devices for Low Light Level Imaging," in Proc. 1973 CCD Applications Conf., pp. 235-245.
2. H. V. Soule, Electro-Optical Photography at Low Illumination Levels, John Wiley and Sons, New York, 1968, pp. 332-333.
3. "Moving Target Sensors," Texas Instruments, Navy Contract N00039-73-C-0070, Final Report, 1973.

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APPENDIX B

Sampled Video Noise Analysis

In order to understand the factors which determine the low light level performance of the TDI array, we will examine the various noise sources which influence the minimum detectable signal called the noise equivalent signal (NES). We will formulate this NES at the output collecting diode which is the input to the on-chip electrometer.

A source of noise exists in the leakage current and the output collection diode shown in Figure 1 accumulates a leakage charge Q_L which consists of leakage in the acrosstrack or TDI direction and the alongtrack or direction of the readout register. If we consider M TDI stages, then the shot noise associated with this leakage charge becomes,

$$\left(\overline{N_n^2}\right)^{1/2} \quad \text{(r.m.s. electrons)} = \left(\frac{J_L A\tau\ (M+1)}{q}\right)^{1/2} \tag{1}$$

where,

J_L = nominal leakage current density ($8nA/cm^2$-$20nA/cm^2$)*

A = sensor area = 76 μm x 76 μm = $5.7 \times 10^{-5} cm^2$

τ = nominal dwell time = 8 μsec

M = number of TDI stages = 9

q = electronic charge = $1.6 \times 10^{-19} C$

Substitution of the above quantities in Eq. (1) we have,

$$\left(\overline{N_n^2}\right)^{1/2} \left[\begin{array}{l}\text{r.m.s. electrons due} \\ \text{to leakage charge}\end{array}\right] = 15\text{-}24e^- \tag{2}$$

*The second of 2 numbers given is the conservative estimate.

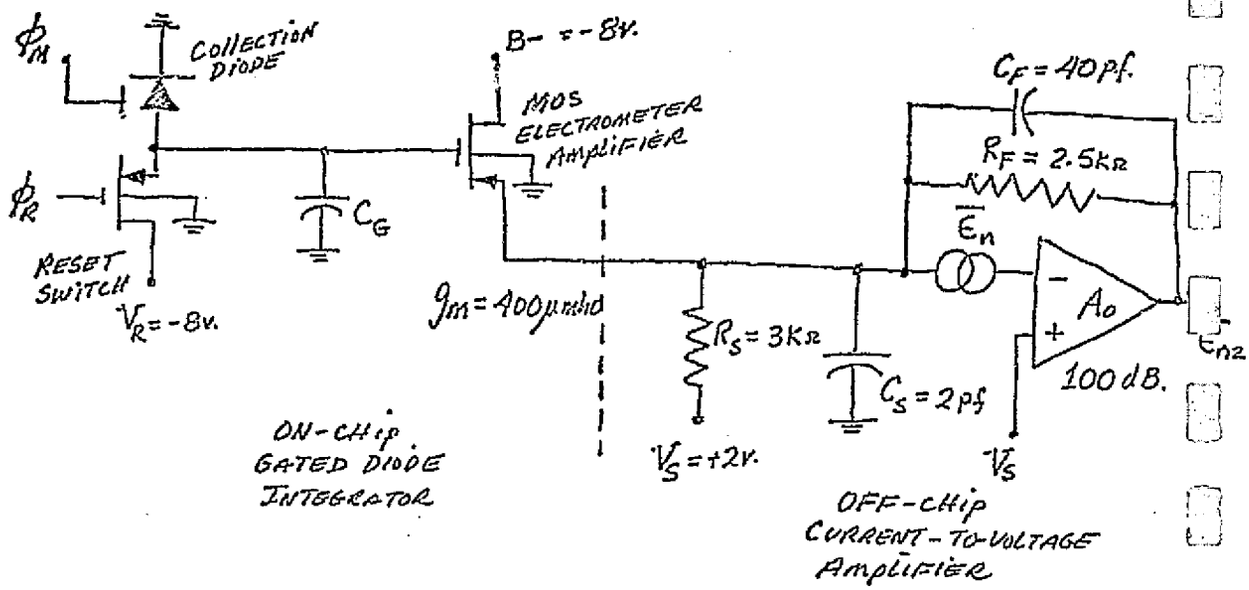

Figure 1. Output Collection Diode, Reset Switch and Electrometer Amplifier of TDI Chip

A second source of noise on the chip is associated with the finite noise resistance of the reset switch which introduces a thermal noise called Johnson-Nyquist noise. The thermal noise is determined by the node capacitance C_G and may be written as,[1]

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} \left\{\begin{array}{l}\text{r.m.s. electrons}\\ \text{of Johnson-Nyquist}\\ \text{thermal noise}\end{array}\right\} = \frac{1}{q}\left(kTC_G\right)^{\frac{1}{2}} \qquad (3)$$

[1] M.H. White, et. al., "Characterization of Surface Channel CCD Imaging Arrays", IEEE Trans. Solid-State Circuits, SC-9, 1, (1974).

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where,

k = Boltzmann's Constant = 1.36×10^{-23} J/°K

T = absolute temperature = 300°K

C_G = node capacitance (approximately 0.15pF for a self-aligned electrometer and reset switch .3pf for non self-aligned)

Substitution of the above values in Eq. (3) yields

$$\overline{N_n^2}^{\frac{1}{2}} \left\{ \begin{array}{l} \text{r.m.s. electrons due} \\ \text{to Johnson-Nyquist} \\ \text{thermal noise} \end{array} \right\} = 155\text{-}219e^- \qquad (4)$$

A third noise source, peculiar to CCD operation, is the trapping and release noise associated with surface and bulk traps. We will assume the CCD is operated in the buried channel mode such that the bulk trapping density determines the noise charge at the collection diode. The noise electrons from this mechanism may be expressed as,[2]

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} \left\{ \begin{array}{l} \text{r.m.s. electrons} \\ \text{from bulk trap} \\ \text{generation/recombination} \end{array} \right\} = \left[NN_T Ad \left(1 - e^{-\frac{\tau}{Np\tau_e}}\right) e^{-\frac{\tau}{Np\tau_e}} \right]^{\frac{1}{2}} \qquad (5)$$

where

N = number of TDI channels per electrometer = 10

N_T = bulk trapping density = $2 \times 10^{11}/cm^3$

A = output register area = sensor area = $5.7 \times 10^{-5} cm^2$

d = depth of ion implantation = 0.2 μm

p = number of electrodes per sensor readout stage = 8

τ_e = emission time constant of traps

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[2] A Study of Noise in Charge-Coupled Devices, S.P. Emmons, et. al., Final Report, May 1975, NRL Contract N00014-74-C-0286. (Texas Instruments-Dallas, Texas).

We do not need to know τ_e in order to estimate the contribution of the bulk trapping noise because we can consider a worst-case analysis which maximizes the noise when

$$\frac{\tau}{Np\tau_e} = \ell n 2 \qquad (6)$$

for maximum use

Substitution of the above values into Eq. (5) under the maximum noise conduction Eq. (6) gives,

$$\overline{N_n^2}^{\frac{1}{2}} \left\{ \begin{array}{l} \text{maximum r.m.s.} \\ \text{electrons from} \\ \text{bulk trapping} \\ \text{effects} \end{array} \right\} = 24\ e^- \qquad (7)$$

A fourth major noise source is the MOS electrometer noise which may be written in the form,[3]

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} \left\{ \begin{array}{l} \text{r.m.s. electrons} \\ \text{due to MOS} \\ \text{electrometer} \end{array} \right\} = \frac{1}{q} \left\{ \overline{G_{nl}^{\ 2}}\, \Delta f_{nl} C_G^{\ 2} \right\}^{\frac{1}{2}} \qquad (8)$$

[3] Solid-State Imaging, Ed. by Jespers, Vonderwiele, and White (Noordhoff-Leyden) 1976.

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where,

$\overline{\varepsilon_{n1}^2}$ = spectral noise voltage density of the p-channel MOS electrometer (W/L = 8:1) measured of the half-power point $\left[\left(\frac{15\text{-}30\text{nV}}{\sqrt{\text{Hz}}}\right)^2 \text{ at 60 KHz}\right]$

Δf_{n1} = noise bandwidth of the electrometer (calculated without correlated-double sampling) = 5.0 MHz.

Substitution of the above values in Eq. (8) yields,

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} \left\{\begin{matrix}\text{r.m.s. electrons}\\ \text{due to MOS}\\ \text{electrometer}\end{matrix}\right\} = 32\text{-}64e^- \qquad (9)$$

Thus, we see the major contribution to on-chip noise is the reset thermal noise and we may write,

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} \left\{\begin{matrix}\text{total on-chip}\\ \text{r.m.s. noise}\\ \text{electrons}\end{matrix}\right\} = \Big[\underbrace{(15e^-)^2}_{\text{leakage}} + \underbrace{(155e^-)^2}_{\text{thermal}} + \underbrace{(24e^-)^2}_{\text{bulk trapping}} + \underbrace{(32e^-)^2}_{\substack{\text{mos}\\ \text{electrometer}}}\Big]^{\frac{1}{2}} = 161\text{-}230e^- \qquad (10)$$

The off chip amplifier contributes noise which may be estimated from Figure 1 and the expression,

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} \left\{\begin{matrix}\text{r.m.s. electrons}\\ \text{from amplifier}\end{matrix}\right\} = \frac{1}{q\, g_m R_F} \left[\overline{\varepsilon_{n2}^2}\ \Delta f_{n2} C_G^2\right]^{\frac{1}{2}} \qquad (11)$$

where,

g_m = transconductance of the electrometer (W/L = 8:1) = 200-400 μmho's at V_R = -8v

Δf_{n2} = noise bandwidth of amplifier (calculated without correlated-double-sampling) = 3.5 MHz

$\overline{\varepsilon_{n2}^2}$ = spectral noise voltage density of the amplifier $\left(\frac{20nV}{\sqrt{Hz}}\right)^2$

R_F = feedback gain resistor = 2.5K

C_F = feedback capacitor = 40pf.

Substitution of the above quantities in Eq. (11) yields,

$$\left(\overline{N_n^2}\right)^{1/2} \quad \left\{\begin{matrix}\text{r.m.s. electrons} \\ \text{from amplifier}\end{matrix}\right\} = 35\text{-}70e^- \tag{12}$$

The other source of accountable off chip noise is due to the random arrival of the incident photons. The photon shot noise may be written as,

$$\left(\overline{N_n^2}\right)^{1/2} = \left[\frac{R_\lambda H_\lambda M \tau}{q}\right]^{1/2} \tag{13}$$

where we have defined responsivity in terms of signal current per "irradiance"

R_λ = responsivity of the sensor $\left(\frac{A}{W/m^2}\right) = q\,\frac{\eta(\lambda) A_D}{hC/\lambda}$

$\eta(\lambda)$ = effective quantum efficiency $\simeq 0.7$

h = Planck's constant = 6.67×10^{-34} J·sec

C = speed of light = 3×10^8 m/sec

λ = wavelength (μm)

A_D = area of detector (m^2)

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Substitution of the above quantities into Eq. (13) yields,

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} = 1206\left(H_\lambda \lambda\right)^{\frac{1}{2}} \left(\begin{array}{c}\text{r.m.s. electrons due} \\ \text{to photon shot noise}\end{array}\right) \qquad (14)$$

where H_λ is the narrow-band irradiance (W/m^2) and $\lambda(\mu m)$ the center wavelength of the band.

The on-chip and off-chip noises may be combined to formulate the signal-to-noise at the collection diode. Thus, combining equations (10), (12) and (14) we have,

$$\frac{S}{N} = \frac{1.45 \times 10^6 H_\lambda \lambda}{\sqrt{1.45 \times 10^6 H_\lambda \lambda + (165 e^-)^2}} \qquad (15)$$

Table 2 illustrates the noise analysis of the TDI-chip for each spectral band. In all the spectral bands the predicted S/N ratio exceeds the specified S/N ratio and the photon-shot noise limits the achievable S/N ratio with the reset noise (on-chip) the second source of major importance. This analysis indicates the proposed TDI array will meet the goals of the Work Statement with regards to low-light level performance. State-of-the-art signal processing at speeds pixel rates of 2.5 MHz is not required.

Table 2. Noise Analysis of TDI-Chip

M = 9 TDI stages — Pixel Size = 76 μm x 76 μm

N = 10 channels/electrometer — τ(dwell time) = 8 μsec

	SPECTRAL BAND nm	IRRADIANCE AT THE DETECTOR H_λ (W/M^2)	S/N (SPEC)	S/N (PREDICTED)	$\left(\overline{N_n^2}\right)^{1/2}$ TOTAL NOISE ELECTRONS	% MARGIN
0	450-520	0.155	105	178-296	345-404	170-28
1	520-600	0.143	145	279-307	379-416	192-212
2	630-690	0.087	105	222-251	333-375	211-23
3	740-800	0.055	85	178-207	298-345	209-244
4	800-910	0.102	120	294-323	393-429	245-26

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APPENDIX C

CORRELATED DOUBLE SAMPLING*

A typical output circuit for a charge coupled device is shown in Figure 1. The gate of the input amplifier is reset by closing, then opening the reset switch after the signal has been read from the previous element. The signal charge from the next element is then transferred to the gate node by actuating the transfer gate, and the signal is then sampled by operating a series switch at the preamplifier output and held for read-out on a shunt capacitor.

The signal voltage at the amplifier input is q_s/C_S. To maximize response, the first amplifier transistor is built on chip to minimize C_S, and is a field effect transistor for high input impedance, and will be called an electrometer amplifier. Since the amplifier measures signal charge, it is simplest to express noise in terms of the equivalent rms charge fluctuation at the gate of the electrometer amplifier. In this circuit, excluding the noise sources within the CCD,

$$q_n = \sqrt{AkTC_S + \varepsilon_{nl}^2 \Delta f_{nl} C_S^2 + \frac{i_{n2}^2 \Delta f_{n2} C_S^2}{g_m^2}}$$

The three noise terms are:

a. The Charge Uncertainty Left After Resetting the Gate Node Capacitance C_S

While the reset transistor switch is closed it forms an RC circuit in which the channel resistance parallels C_S. The

*This section is taken from "Amplifier and Amplifier Noise Considerations" by Dr. J. A. Hall, a chapter in the Look "Solid State Imaging". Dr. Hall is a member of the Westinghouse team assigned to this program.

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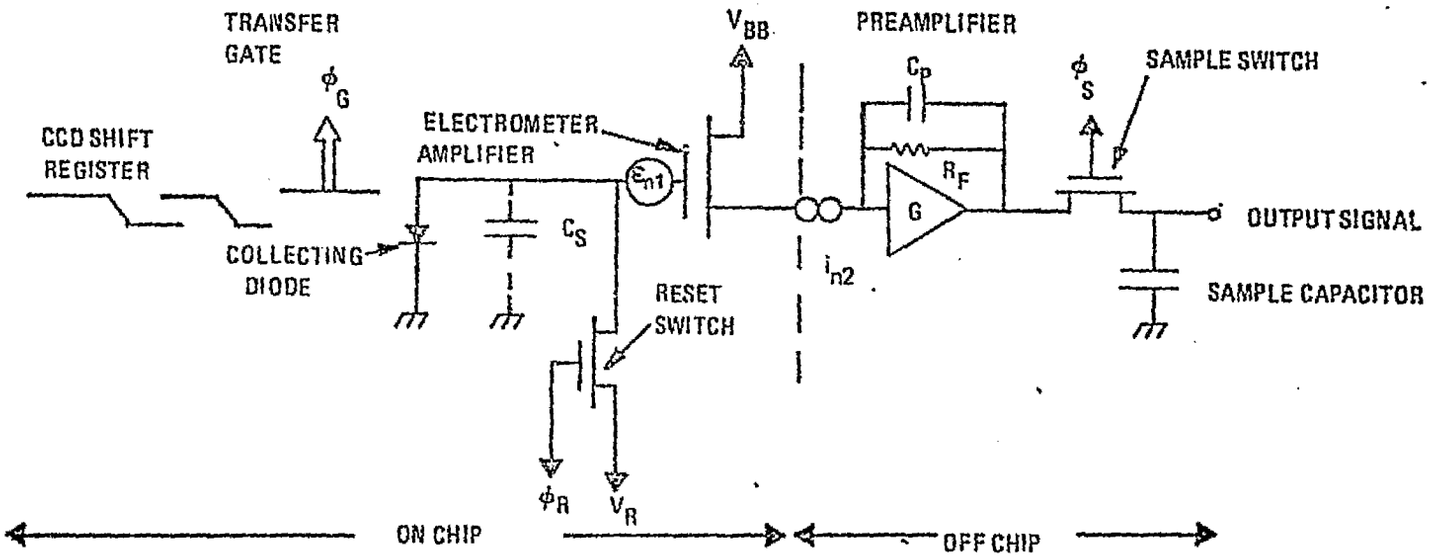

Figure 1. For a Simple Sampled and Reset Amplifier Input, the Principal Noise Source is Johnson Noise in the Reset Switch

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channel resistance Johnson noise spectrum is band limited by the parallel combination. The instantaneous value of the noise charge at the moment the switch opens is left on the capacitor to be added to the next signal charge transferred to the electrometer gate node. If the reset switch has no excess noise, $q_n = \sqrt{kTC_S}$. Measurements indicate typical MOS transistor switches may have up to $\sqrt{2}$ times this value. This term corresponds directly to the load resistor Johnson noise in the camera tube preamplifier.

b. The First Stage Amplifier Noise

The first electrometer amplifier stage is invariably a field effect transistor, whose noise can be well represented as shown by a noise voltage generator, ε_{nl} internal to the transistor in series with the gate. This noise voltage appears amplified at the off chip preamplifier output, band limited at Δf_{nl} by the preamplifier, and its instantaneous value is added to the signal and sampled and held when the sample switch is opened. The preamplifier gain is assumed to be large enough so that noise in the sample switch is insignificant. The mean sqaure of the equivalent input noise charge is $\varepsilon_{nl}^2 \Delta f_{nl} C_S^2$ and if there is no significant excess 1/f noise in the amplifier passband, ε_n is simply the mid band noise voltage. If the passband includes a significant 1/f contribution, one can evaluate the

integral $\frac{1}{2\pi \varepsilon_{nl}^2} \int_{2\pi f_1}^{2\pi f_2} \varepsilon_n^2(\omega)\, d\omega = \Delta f_n$ to determine an effective noise bandwidth.

c. The Noise Contribution of the Following Off Chip Stages

This term is expressed separately because the amplifier is usually off chip and can be measured separately, and because the on chip electrometer amplifier stage will often have a low enough transconductance so that off chip noise contributions are significant. This term is meaningful for a specific amplifier configuration, and here we will assume a current mode input operational amplifier with an effective input noise of 2.6×10^{-12} amp. Again C_S must be minimized to minimize this noise component.

To consider a specific example, consider a CCD chip with a P-channel MOSFET on chip input amplifier. Let:

$$C_S = 0.25 \text{ pF}$$

$$\varepsilon_{n1} = 20 \times 10^{-9} \text{ V/Hz}^{1/2}$$

$$\Delta f_{n1} = \Delta f_{n2} = 1 \times 10^{6} \text{ Hz}$$

$$A = 2$$

$$i_{n2} = 2.6 \times 10^{-12} \text{ amp/Hz}^{1/2}$$

$$g_m = 150 \text{ } \mu\text{mho}$$

Then $q_n = \sqrt{2 \times 10^{-33} + 2.5 \times 10^{-35} + 1.85 \times 10^{-35}}$ coul = 283 electrons

Thus most of the equivalent input noise is reset switch Johnson noise, at least at this comparatively low data rate.

To remove most of the reset noise contribution, Westinghouse engineers have developed correlated double sampling.[1] Unlike most noise contributions,

[1] White, M.H., et al, U.S. Patent 3,781,574

reset noise is sampled and held on C_S at the moment the reset switch is opened. If leakage to the electrometer gate node is small, it is possible to read this reset noise before the next signal charge packet is transferred and to separate signal from noise. A mechanization is shown in Figure 2. After the reset switch has opened, a clamp switch closes at the output of the preamplifier to store the negative of the amplified reset noise charge on the coupling capacitor. The clamp switch then opens, sampling the electrometer and preamplifier transistor noise and holding this sample also on the clamp capacitor. The next signal charge packet is then transferred to the gate node of the on chip electrometer amplifier. The voltage at the preamplifier output is now the amplified signal plus the amplified reset noise plus the sampled transistor and amplifier noise plus the on going time varying transistor and amplifier noise. The voltage at the output of the clamp capacitor is the sum of amplified signal plus sampled electrometer transistor plus amplifier noise plus the on going transistor and amplifier noise. The reset noise has been removed. The transistor sample switch is then closed and opened, holding at the output the sum of the amplified signal plus two independent samples of electrometer transistor and preamplifier noise. The second amplifier noise sample was taken at the instant the sample switch was opened. As shown in the example, the reset noise was an order of magnitude larger than the amplifier noise and its removal is important despite the double sampling of amplifier noise.

Correlated double sampling has other advantages, however, since the clamp and sample operations are performed within a single element time, usually only one or a few microseconds apart. The system output voltage is the difference in instantaneous preamplifier output voltage between these two samples, which

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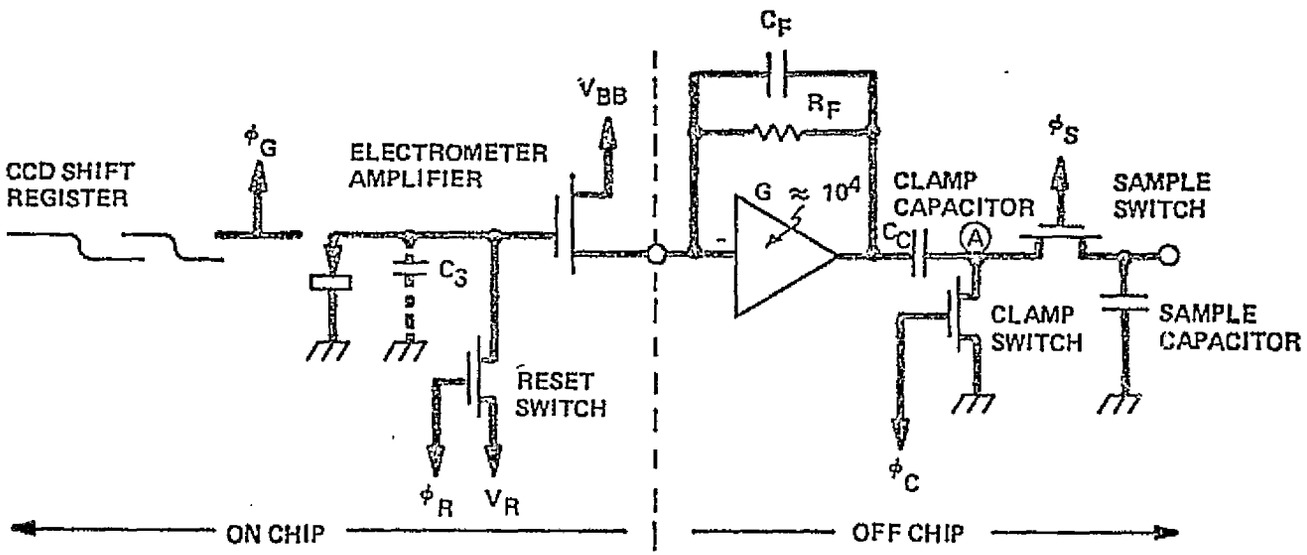

Reset switch replaces load resistor for CCD. Correlated double sampling shown removes most of reset switch Johnson noise, leaving CCD noise, electrometer amplifier noise, and off-chip amplifier noise. C_S is still a performance determining factor.

C.D.S. Operations:

1. Reset diode node to $V_R \pm \sqrt{kTC_S}$
2. Close clamp switch so negative of reset noise sample appears across C_C. Open clamp switch.
3. Transfer next signal charge packet to gated collection diode.
4. Signal at (A) is $f[(q_s + q_n) - q_n] = f(q_s)$ alone. Operate sample switch to present corresponding signal at output.

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Figure 2. Correlated Double Sampling Removes Reset Noise at CCD Output.

effectively provides ac coupling to neglect any frame rate or quasi-dc level shifts at the chip output. The effective frequency response of this system for a 2 microsecond delay between the opening of the clamp and sample switches is shown in Figure 3. The response at zero frequency is zero, and is very low at low frequencies to greatly reduce the effect of excess 1/f noise in the electrometer amplifier, the off chip preamplifier, or the power supplies.

With correlated double sampling the amplifier noise equation becomes:

$$q_n = \sqrt{\varepsilon_{n1}^2 \Delta f_{n1} C_S^2 + \frac{i_{n2}^2 \Delta f_{n2} C_S^2}{g_m^2}}$$

where Δf_{n1} is now roughly twice the analog bandwidth of the operational preamplifier to represent the two noise samples. For the same on chip components used above

$$\varepsilon_{n1} = 20\times10^{-9}\ \mathrm{V/Hz^{1/2}} \qquad i_{n2} = 2.6\times10^{-12}\ \mathrm{amp/Hz^{1/2}}$$

$$\Delta f_{n1} = 2\times10^{6}\ \mathrm{Hz} \qquad \Delta f_{n2} = 2\times10^{-6}\ \mathrm{Hz}$$

$$C_S = 0.25\times10^{-12}\ \mathrm{fd} \qquad g_m = 150\ \mu\mathrm{mho}$$

$$q_n = \sqrt{5\times10^{-35} + 3.76\times10^{-35}} = 58 \text{ electrons.}$$

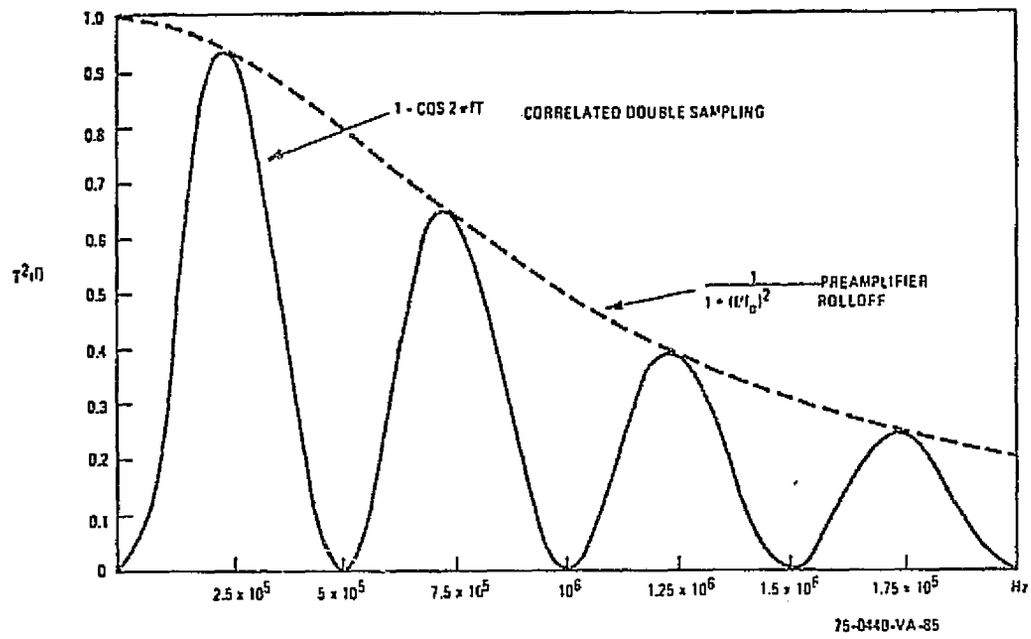

Figure 3. Effective Frequency Response of a CDS System with 2 μsec Between Opening of Clamp and Sample Switches.

Thus with correlated double sampling a realistic CCD output circuit and amplifier embodiment should give noise of less than 60 electrons with an amplifier noise bandwidth of 1 MHz, raised to an effective bandwidth of 2 MHz by the double sampling of amplifier noise. Since q_n = const x $\Delta f^{1/2}$, correlated double sampling can give even lower noise at lower data rates. On the other hand, at data rates of 5 to 10 MHz required for full resolution television imaging with brute force interlacing, $q_n \approx$ 131 to 185 electrons, large enough to rule out desirable low light level performance.

What can be done to reduce this figure? As shown earlier in this chapter, $\epsilon_n \propto g_m^{-1/2}$ and $g_m \propto C_{AG}$, the active gate capacitance. As before, the active gate capacitance should be matched to the capacitance of the CCD output circuit, after that has been minimized as far as possible. But the collection diode and

reset switch diffusion and the interconnecting and overlap capacitances total about 0.1 pF even with careful design, and at 0.25 pF C_S seems within a factor of two of the bare minimum. ε_n cannot be made much smaller for an electrometer transistor with such a small active gate capacitance. The approach used in camera tube type equipment was to parallel input transistors to increase g_m and lower ε_n. If this could be done without increasing C_S proportionally, one could reduce first stage noise significantly, and also provide enough first stage signal gain so that the effect of off chip preamplifier noise was significantly reduced.